1. (2 points) Of the three following hardware/software partitioning approaches, tightly-coupled coprocessor, loosely-coupled coprocessor, and instruction set extensible processor, what type of approach is utilized within the Chimaera processor design. Very briefly define one positive and one negative aspect of this approach compared to the other listed approaches.

2. (3 points) Partitioning the following C code to a loosely-coupled coprocessor design. Using the profile information annotated within C code, determine which of the two innermost loops will result in the best increase in performance when partitioned to a hardware coprocessor. Partition the selected innermost loop to hardware and estimate the speedup of the partitioned design over software only execution.

```c
int main() // Total Cycles: 8193437
{
    int n;
    int i, j, k;
    for (n = 0; n < LOOPS; n++) // Total Cycles: 8186006, Execs: 1, Iters: 1000
    {
        for (i=1; i<=SIZE; i++) // Total Cycles: 579000, Execs: 1000, Iters: 5
            for (j=1; j<=SIZE; j++)
                c[i][j] = 0;
        for (i=1; i<=SIZE; i++) // Total Cycles: 7579000, Execs: 1000, Iters: 5
            for (j=1; j<=SIZE; j++)
                for (k=1; k<=SIZE; k++) // Total Cycles: 7225000, Execs: 25000, Iters: 5
                    c[i][j] += a[i][k] * b[k][j];
    }
    return 0;
}
```