Analog to Digital Converter
- Input is analog signal
- Output is binary number
- Speed is the time to convert
- Unipolar/Bipolar conversion

Principles
- See Text on Elmo, Whiteboard

Sensors

Analog to Digital
**Terminology**

- Precision: number of distinguishable levels
- Resolution: smallest distinguishable change
- Range: maximum and minimum on measured signal
- Accuracy: (actual-ideal)/ideal

**MUX**

- Usually multiple input can be selected (MUX) and an analog sample and hold circuit is integrated before the ADC.

**Nyquist**

- Will need to sample 2 times the maximal frequency in your signal
- Will need to low-pass filter analog signal before conversion with $f_c$ at least at half the sampling frequency
- Will need to select $f_c$ larger than the maximal frequency in signal of interest

**1bit A/D Converter**
Comparator

- Most comparators have open collector transistor output
- 311 operates on single 5 Volt
- Pull up to 5 V

Comparator with Hysteresis

- Want to prevent bouncing
- Added positive feedback to generate hysteresis

2 Bit Flash ADC

Ramp ADC

Counter Type

CLK inputs into counter which sequentially increases until DAC output matches input which stops Counter
8 bit RAMP ADC

This works like the counter type but a programmer drives the DAC by successfully dividing the measurement range. First MSB is determined, last is the LSB. This is fast and has high resolution.

HCS12 A/D Converter

- 8/10 bit resolution
- 7 microseconds for 10 bit
- 8 channel MUX
- Signed or Unsigned numbers
- Single or Continuous conversion

ADC

Successive Approximation

This works like the counter type but a programmer drives the DAC by successfully dividing the measurement range. First MSB is determined, last is the LSB. This is fast and has high resolution.

Figure 8-1, ATD18B3C Block Diagram
### Pins
- AN0..AN7
- VRH,VRL
- VDDA, VSSA

### Data Registers
- ATD0..7

### Control/Status Registers
- **ATDCTL2**
  - ATD power up,
  - AFFC clear,
  - AWAI power down in wait mode,
  - External Trigger Edge,
  - External Trigger polarity,
  - External Trigger enable,
  - ATD Sequence Complete Interrupt,
  - ATD Sequence Complete Flag

- **ATDCTL3**
  - Conversion sequence length 1..8, S1,2,4,8

- **ATDCTL4**
  - Speed

- **ATDCTL5**
  - Input select code (how many)
  - Continuous
  - Data justification/representation
Control/Status Registers

- ATDIEN
  - Input enable

Status Registers

- ATDSTAT0
  - Sequence complete
  - External trigger under run

- ATDSTAT1
  - Conversion complete (for each channel)

Digital to Analog Converter

Digital to Analog
DAC Versions

Example R-2R Implementation

Output

Old Material Here After

Unsigned: $V_{\text{out}} = V_{\text{dc}}\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16} + \frac{b_4}{32} + \frac{b_5}{64} + \frac{b_6}{128} + \frac{b_7}{256}\right) + V_{\text{dc}}$

Signed 2's complement: $V_{\text{out}} = V_{\text{dc}}\left(-\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16} + \frac{b_4}{32} + \frac{b_5}{64} + \frac{b_6}{128} + \frac{b_7}{256}\right) + V_{\text{dc}}$
**Example DAC for HC11**

**Filters**

**Analog Signal Filter**
- One pole with inverting amplifier (low pass)
- \( f_c \) at 0.707 of original throughput value

\[
V_{out} = -\frac{V_{in}}{1 + j\omega R_2 C} \quad \omega = \frac{1}{2\pi R_2 C} \\
R_3 = \frac{R_1 + R_2}{R_1 + R_2}
\]

**Two pole Low Pass**
- Butterworth Filter
- Capacitors maintain 2/1 ratio

\[
\frac{V_{out}}{V_{in}} = \sqrt{1 + \left(\frac{f}{f_c}\right)^4}
\]
Design Steps

1. Select the cutoff frequency $f_c$
2. Divide the two capacitors by $2\pi f_c$ (let $C_{1A}$, $C_{2A}$ be the new capacitor values)
   
   $C_{1A} = \frac{141.4 \text{ } \mu F}{2\pi f_c}$
   $C_{2A} = \frac{70.7 \text{ } \mu F}{2\pi f_c}$
3. Locate two standard-value capacitors (with the 2/1 ratio) with the same order of magnitude as the desired values; let $C_{1B}$, $C_{2B}$ be these standard value capacitors and let $x$ be this convenience factor
   
   $C_{1B} = \frac{C_{1A}}{x}$
   $C_{2B} = \frac{C_{2A}}{x}$
4. Adjust the resistors to maintain the cutoff frequency
   
   $R = 10 \text{ k}\Omega \cdot x$

Two pole High Pass

- Butterworth Filter
- Resistors maintain 2/1 ratio

$$V_{out} = \frac{\left(\frac{V_{in}}{V_{in}}\right)^4}{1 + \left(\frac{f}{f_c}\right)^4}$$

Design

1. Select the cutoff frequency $f_c$
2. Divide the two capacitors by $2\pi f_c$ (let $C_A$ be the new capacitor value)
   
   $C_A = \frac{1 \text{ } \mu F}{2\pi f_c}$
3. Locate a standard value capacitor with the same order of magnitude as the desired value; let $C_B$ be this standard value capacitor and let $x$ be this convenience factor
   
   $C_B = \frac{C_A}{x}$
4. Adjust the two resistors to maintain the cutoff frequency
   
   $R_1 = 707 \text{ k}\Omega \cdot x$
   $R_2 = 1414 \text{ k}\Omega \cdot x$

HC11 AD converter

- All capacitative charge redistribution method
- 8 bit
- Up to 8 channel (not all connected in DIP)
**HC11 A/D pins**

- PB3/A11: 12
- PB2/A10: 14
- PB1/A9: 15
- PB0/A8: 16
- PE2/AN2: 19
- PE3/AN3: 20
- PE2/AN1: 18
- PE1/AN0: 17

**ADPU** turn on/off charge pump for switching transistors. 7.8 V needed.

**CSEL** turn on/off internal oscillator for A/D converter, uses normally E clock but if E clock is set very low will need different oscillator.

**HC 11 A/D converter OPTION**

| Address: | $1039 |
| Read:  | ADPU | CSEL | IROE | DLY | CME | --- | CR1 | CR0 |
| Write: | | | | | | | | |
| Reset: | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |

**HC11 A/D Status and Control**

- CCF conversion complete flag (read only)
- Scan 1=continuous conversion, 0 4 conversion
- MULT 0=convert each channel, 1=convert one channel 4 times
- CD,CC (0,0) channel 1..4, (0,1) channel 5..8
- CB,CA (0,0)channel 1, (0,1) channel 2 etc.
- IF YOU WRITE TO THIS REGISTER YOU WILL START CONVERSION

**HC11 A/D Results Registers**

- ADR1..ADR4, 8 bit registers, if CCF is high results are valid

**Address:** $1030

<table>
<thead>
<tr>
<th>Bit 7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CCF</td>
<td>0</td>
<td>SCAN</td>
<td>MULT</td>
<td>CD</td>
<td>CC</td>
<td>CB</td>
<td>CA</td>
</tr>
</tbody>
</table>

**Reset:** U - Unaffected
HC11 A/D Sampling (4bits shown)

Assume $V_L=0$

Accumulated charge in all capacitors: $Q=16^*V_x$

HC11 A/D Hold (4 bits shown)

$V_i=-V_x$

HC11 A/D Conversion (4bits shown)

Different Capacity

Can set to $V_L$ or $V_H$

Example Conversion

- Assume $V_x = 21/32^*V_H$
- $V_x$ always $\leq V_H$
- When sampled the capacitors got charged
  $Q=16^*V_x$, therefore
  $Q=21/2^*V_H$
Conversion 1st Step

\[ Q = 8(VH-V_i) + 8(VL-V_i), \]
\[ VL = 0, \]
\[ Q = \text{original charge of } 21/2 \text{ VH} \]

Therefore \( V_i = -5/32 \text{ VH} \)
Output of the comparator will be 1
Therefore the switch for Capacitor 8 will stay

Conversion 2nd Step

\[ Q = 8(VH-V_i) + 4(VH-V_i) - 4(=2+1+1) V_i \]
\[ VL = 0 \]
\[ Q = 21/2 \text{ VH} \]

Therefore \( V_i = 3/32 \text{ VH} \)
Output of the comparator will be 0
Therefore the switch for Capacitor 4 will not stay

Conversion 3rd Step

\[ Q = 8(VH-V_i) + 2(VH-V_i) - 6(=4+1+1) V_i \]
\[ VL = 0 \]
\[ Q = 21/32 \text{ VH} \]

Therefore \( V_i = -1/32 \text{ VH} \)
Output of the comparator will be 1
Therefore the switch for Capacitor 2 will stay

Result

- 8 is on
- 4 is off
- 2 is on
- 1 is off

- 1 0 1 0 binary = 10 decimal
- \( V_x = 10/16 \times \text{ VH} \)
- But we said that \( V_x = 21/32 \text{ VH} \)!
- Have additional bit/capacitor for \( 1/2 \) LSB quantization error
- 1 0 1 0 1 binary = 21 decimal.
Actual weighted circuit used

ADC

1 Bit Approach

- Can use a 1 bit DAC running a much higher frequency than the actual A/D conversion speed
- Sigma Delta ADC
Sigma Delta