Structure of Microprocessor Systems

The System Bus contains:
- Address Bus, unidirectional
- Data Bus, bi-directional
- Control Lines

- ADDRESS: tells which module (RAM, ROM, IO) interacts with the processor
- DATA: information to be transferred from/to processor to/from other devices
- CONTROL: specifies direction (read, write) and when transfer takes place
**Bus Cycle**

- A bus contains address, data and control information
- A complete data transfer is a bus cycle
- HC11/2 has two types of transfers:

<table>
<thead>
<tr>
<th>Type</th>
<th>Address driven</th>
<th>Data driven</th>
<th>Transfer</th>
</tr>
</thead>
<tbody>
<tr>
<td>Read cycle</td>
<td>Processor</td>
<td>RAM ROM Input</td>
<td>Data copied to processor</td>
</tr>
<tr>
<td>Write cycle</td>
<td>Processor</td>
<td>Processor</td>
<td>Data copied to RAM or Output</td>
</tr>
</tbody>
</table>

**Memory Mapped Architecture**

- RAM, ROM and IO is connected to processor in a similar way
- I/O devices are assigned a memory address
- Reading from memory or I/O uses same instructions
- Writing to memory or I/O uses same instructions
- HCS12 uses a 16 bit address bus: 64kbyte map range
- HCS12 uses a 16 bit data bus: 2 bytes accessed at once
Expansion Buses for Microcontroller

- Serial
  - synchronous
  - asynchronous
  - I²C
  - MCAN
- Parallel with DI/O
- Parallel with standardized Bus
  - ISA 8/16 bit, 4.77 MHz
  - PCI 32/64bit, 33/66MHz

Bus Collision Management

- Normally there are multiple IO resources attached on system bus
- Master and Slave Arbitration if IO Resources act independently
- Needs Control Algorithms
  - Static time multiplexing (fixed time slot for each unit)
  - Dynamic time multiplexing with central control (e.g. CPU internal)
  - Dynamic time multiplexing with distributed control (e.g. Ethernet)

General Processor

General Bus Timing Diagram

Master activates addresses, indicates require operation (read), activates MSYN
Slave puts data on data bus, activates SSYN
Master reads data and acknowledges by deactivating MSYN
Example Expanded Mode Bus Timing

Address valid

Data valid

Data transfer finished

Multiplexed Bus with HCS12
Wide Data/Address Bus

2*8 Bit I/O resources

PB PA
ECLK

Address Bus

CS
Low Byte

D
R/W
OE*

HC 12