A Frequency Synthesizer With Optimally Coupled QVCO and Harmonic-Rejection SSBmixer for Multi-Standard Wireless Receiver

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***Abstract*—This paper presents a wide-band fractional-N frequency synthesizer for multi-standard cellular and short-range wireless communication receivers. The synthesizer covers the frequency band from 1.8 to 6 GHz and supports the standards of DCS1800, WCDMA, TD-SCDMA, WLAN802.11 a/b/g and Bluetooth. Architecture design and frequency planning are carefully performed to tradeoff wide frequency range and power efficiency. A quadrature voltage-controlled oscillator (QVCO) with a new phase shifter scheme is developed which shows better phase noise performance and more stable oscillation. Combining harmonic rejection and single sideband mixing, a harmonic-rejection SSBmixer (HR-SSBmixer) is developed to suppress unwanted sidebands and spurious signals. It serves as a power-saving solution to generate the LO signal for the 802.11a mode by avoiding power-hungry poly-phase filters or high-frequency LO buffers and dividers. The synthesizer is designed in a 0.13-μm CMOS technology. It occupies an active area of 1.86 mm^2 and consumes 35.6 to 52.62 mW of power. Measurement results show that the synthesizer is able to provide in-phase and quadrature-phase (I/Q) signals supporting the standards mentioned above.**

***Index Terms*—Automatic frequency control, frequency synthesizer, harmonic rejection, multi-standard wireless communication, phase noise, QVCO, single sideband mixer.**

I. Introduction

ONE OF THE MAJOR trends of wireless communication is the chip-level integration of multiple communication standards in a low-cost technology. The demand for integrating multiple wireless standards into a single reconfigurable radio is growing together with the proliferation of wireless communication standards. Simply implementing such a radio device with multiple dedicated front-ends integrated in parallel is not a viable solution since power consumption and die area and thus system cost will be unaffordable. The more desirable solution is a flexible multi-standard radio system with high reconfigurability and programmability. One of the challenging blocks of such a reconfigurable radio is the frequency synthesizer that needs to generate clean and stable LO signals fulfilling the requirements of the major wireless communication standards. In [1]–[5], fractional-N frequency synthesizers for generating carrier frequencies covering major communication standards such as GSM, WCDMA, WLAN and Bluetooth have been developed. However, they require multiple VCOs, power-hungry poly-phase filters or high-frequency LO buffers and dividers.

This paper presents another frequency synthesizer [6] designed in a 0.13-μm CMOS technology for multi-standard wireless receivers that support communication standards including DCS1800, WCDMA, TD-SCDMA, Bluetooth, and WLAN 802.11a/b/g. Architecture design and frequency planning are carefully performed to tradeoff wide frequency range and power efficiency. A QVCO is used in the proposed frequency synthesizer. Conventional QVCO, however, suffers from the problems of bimodal oscillation and poor phase noise. To improve the QVCO's performance, the introduction of phase shifters to the coupling stage [7], [8] or the use of capacitive coupling instead of transistor coupling [9] have been previously proposed. The use of a phase shifter in the coupling stage is preferred in this design because capacitive coupling requires more than two LC oscillator stages to ensure a well-defined oscillation mode [9]. In this paper, we propose a new phase shifter scheme which effectively eliminates the bimodal oscillation and at the same time significantly improves the QVCO phase noise and the output phase accuracy. In addition, by combining harmonic rejection and single sideband mixing, a harmonic-rejection single-sideband (SSB) mixer is developed to suppress unwanted sidebands and spurious signals. It serves as a power-saving solution to generate the LO signal for 802.11a by avoiding power-hungry poly-phase filters or high-frequency LO buffers and dividers.

In Section II, we discuss the proposed $\Sigma\Delta$ fractional-N frequency synthesizer architecture and the frequency planning. In Section III, we present circuit design techniques for the quadrature VCO with the proposed phase shifter, the HR-SSBmixer, an automatic frequency control (AFC) circuit as well as a robust programmable frequency divider. Experimental results are discussed and summarized in Section IV.

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TABLE I
SPECIFICATIONS FOR THE MULTI-STANDARD FREQUENCY SYNTHESIZER

Standards	DCS1800	WCDMA	TD-SCDMA	Bluetooth	802.11b	802.11a	802.11g
Frequency Range/MHz RX	1805~1880	2110~2170	1880~1920 2010~2025 2300~2400	2400~2484	2400~2483.5	5150~5350 5725~5850	2400~2484
Channel Spacing	200 kHz	5 MHz	1.6 MHz	1 MHz	25 MHz	20 MHz	25 MHz
Frequency Accuracy	0.1 ppm	0.1 ppm	0.1 ppm	75 kHz	25 ppm	20 ppm	25 ppm
Phase Noise (dBc/Hz)	-119@0.6 MHz -129@1.6 MHz -136@3 MHz	-108.8@7.6 MHz -120.8@15 MHz -150@130 MHz	-111@3.2 MHz -123@5 MHz	-81@1 MHz -111@2 MHz -121@3 MHz	-90@10 kHz -121@14 MHz	-90@10 kHz -100.2@20 MHz -116.2@40 MHz	-90@10 kHz -100.2@20 MHz -116.2@40 MHz
Spur (dBc)	-66@0.6 MHz -76@1.6 MHz -83@3 MHz	-43@7.6 MHz -55@15 MHz	-50@3.2 MHz -62@5 MHz	-21@1 MHz -51@2 MHz -61@3 MHz	-49.5@14 MHz	-28@20 MHz -44@40 MHz	-28@20 MHz -44@40 MHz
Settling Time	865 μs	NA	NA	229 μs	NA	NA	NA

II. ARCHITECTURE DESIGN AND FREQUENCY PLANNING

A. Synthesizer Specifications

The synthesizer specifications typically include frequency range, phase noise, spur and settling time requirements. The proposed $\Sigma\Delta$ fractional-N frequency synthesizer is designed for a direct conversion receiver and supports standards including DCS1800, WCDMA, TD-SCDMA, Bluetooth, and WLAN 802.11a/b/g. The synthesizer thus needs to cover a frequency range from 1.8 GHz to 5.9 GHz. Adjacent channel selectivity (ACS) and blocking characteristics of the receiver set the LO phase noise and spur requirements. Due to the strong power allowed for adjacent channels and the requirement of a large signal-to-noise ratio (SNR), cellular communications such as DCS1800 have very stringent spot phase noise and spur requirements. As shown in Table I, to ensure that the reciprocal mixing is kept below the noise floor, the phase noise for DCS1800 at 3 MHz offset has to be less than -136 dBc/Hz. The WCDMA standard uses direct sequence spread spectrum, the SNR and the spot phase noise requirements can be relaxed. However, WCDMA is a frequency division duplex (FDD) system. For UTRA-FDD Band I, the Tx and Rx bands are 130 MHz apart. The Tx leakage at the receiver input can mix with the receiver LO signal. The phase noise is thus usually set to be less than -150 dBc/Hz at 130 MHz offset to minimize the reciprocal mixing effect [10]. Wideband communication systems such as WLAN, on the other hand, occupy a much larger bandwidth and therefore the LO phase noise specification is often set by the integrated phase noise which is determined by the phase-locked loop (PLL) close-in phase noise. Assuming that the phase noise is constant within the PLL bandwidth ($f_{\mathrm{BW,PLL}}$) and then decreases by -20 dB/dec, the double sideband integrated phase noise $P_{\mathrm{pn,int}}$ can be approximated as

$$P_{\mathrm{pn,int}}|_{\mathrm{dBc}} = 10\log(\pi f_{\mathrm{BW,PLL}}) + L(f_{\mathrm{in}}) \tag{1}$$

where $L(f_{\mathrm{in}})$ is the PLL close-in phase noise in dBc/Hz, and $P_{\mathrm{pn,int}}$ should be larger than the required SNR. Equation (1) sets the RMS phase noise requirements for Bluetooth and 802.11b. For 802.11b, the 11 Mb/s operation mode sets the most stringent receiver specification and the required SNR is 11.5 dB [10]. In the case of Bluetooth, the specified 10^{-3} maximum bit-error rate (BER) can be achieved with a 21 dB SNR [10]. For OFDM system such as 802.11a/g, the LO phase noise will cause inter-carrier interferences and the phase noise specification is derived from numerical simulations. Typically, one leaves enough design margin and sets $P_{\mathrm{pn,int}} = -35$ dBc, which is integrated from 10 kHz to 10MHz [11], and this results in a RMS phase noise of 1° and a close-in phase noise of -90 dBc/Hz with $f_{\mathrm{BW,PLL}} = 100$ kHz. The out-of-band phase noise specification for WLAN is determined by the blocking characteristics and is listed in Table I. One can find that the toughest phase noise requirement for WLAN is the close-in phase noise. In summary, the specification of close-in phase noise of our frequency synthesizer is set by the WLAN standards and the out-of-band phase noise requirement is set by the cellular standards such as DCS1800 and WCDMA.

Settling time of the frequency synthesizer is determined by the PLL loop bandwidth. The settling time for a synthesizer in a

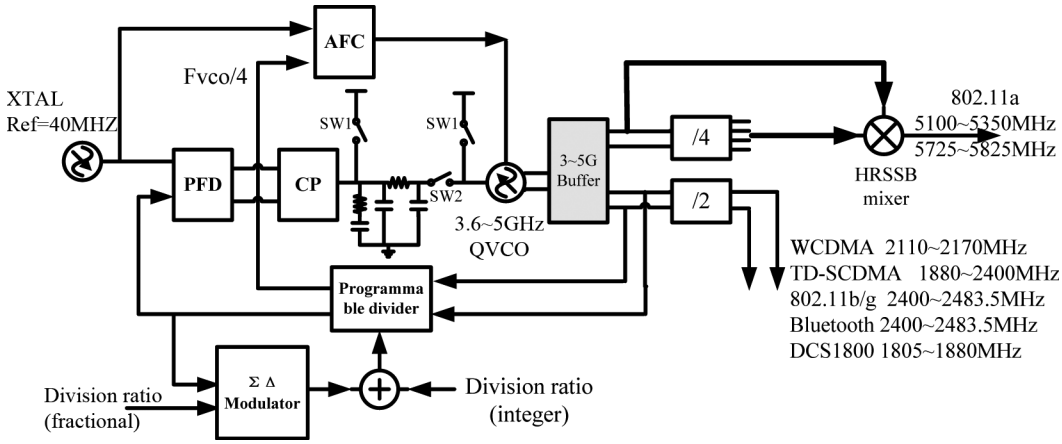

Fig. 1. A block diagram of the proposed multi-standard frequency synthesizer.

time division multiplexed (TDM) cellular system such as GSM is often set by the time required between adjacent transmission packets. In GSM, the most critical switching time for the LO to take place is between the transmission and the system monitoring slots and is about 865 μs. It should be mentioned that not every standard requires a specification on the settling time. For example, in direct-sequence spread spectrum (DSSS) WLAN transceivers, if the transmitter and the receiver share the same LO signal and adopt the same architecture, then there is no need to specify settling time for the synthesizer. We summarize the synthesizer design specifications in Table I. In the table, a 3-dB design margin has been assigned for the SNR when deriving the phase noise and the spur requirements.

B. Synthesizer Architecture and Frequency Planning

According to the design specifications, the synthesizer needs to provide I/Q LO signals over a frequency range from 1.8 GHz to 5.9 GHz. A single VCO alone cannot achieve such a wide frequency tuning range with a reasonable phase noise. Also in direct conversion architecture, it is desirable to set the receiver LO frequency apart from the transmitter operating frequency to avoid LO pulling. One common method to achieve wideband frequency synthesis is to use multiple VCOs with a set of frequency dividers [2]–[4]. The advantage of this synthesizer architecture is its simplicity and good spur performance. However, multiple VCOs can be very sensitive to parasitic capacitance; the VCO and the VCO buffers which operate at twice the LO frequency and the high frequency dividers can all consume a significant amount of power. This approach is a practical solution only when advanced technologies such as 45 nm CMOS [2], 40 nm CMOS [3] and BiCMOS [4] are adopted. Operating the VCO at the LO frequency in combination with dividers and mixers is proposed in [1] and [5] . A drawback of such an approach is that the mixing will generate spurs due to input harmonics. As the multi-standard receiver is a wideband system, the spurs in the LO signal can cause SNR degradation via reciprocal mixing. To reduce the spurious tones, in [5] SSB mixers are used with quadrature inputs generated by a polyphase filter. Furthermore, in [5] input components to the SSB mixer are first linearized by filtering out the third-order harmonic through another polyphase filter. Passive polyphase filter in wideband systems often adopts multi-level configurations. As a result, multiple power-hungry buffers need to be inserted to compensate the power loss. This causes significantly more power consumption and greatly degrades the overall power efficiency of the synthesizer. In addition, the spur performance even with polyphase filtering is rather poor. The reported spur performance in [5] is less than -30 dBc.

The frequency synthesizer reported in this paper is based on an $\Sigma\Delta$ fractional-N PLL, as shown in Fig. 1. The fractional-N architecture allows an arbitrary output frequency resolution, and is appropriate for multi-standard wireless applications. Since the direct conversion topology is adopted, the synthesizer needs to generate quadrature LO signals for complex signal processing. As previously discussed, the CMOS process technology and the communication standards to support play an important role in choosing the synthesizer architecture. The synthesizer is designed in a 0.13-μm CMOS technology, and the highest LO frequency required is from 5.15 to 5.85 GHz set by the 802.11a standard. If using the divide-by-2 approach [2]–[4], the VCO needs to operate up to 11.7 GHz. Both the tuning range and the power consumption are issues in this approach as the high-frequency VCO and its buffers as well as the high-frequency dividers significantly lower the overall synthesizer power efficiency. Therefore, in the proposed synthesizer, a QVCO operating at the LO frequency is adopted. The QVCO is designed to have a tuning range from 3.6 GHz to 5.0 GHz. For the WCDMA, GSM, TD-SCDMA, WLAN 802.11b/g and Bluetooth standards, the LO signals are generated by a divide-by-2 circuit following the QVCO. As shown in Table I, standards including WCDMA, GSM, TD-SCDMA and Bluetooth have very stringent LO spot phase noise and spur requirements. It is unacceptable to use the Divide and Multiply in Quadrature approach as developed in [5] to generate their LO frequencies. To generate the LO signal for WLAN 802.11a, an SSBmixer combined with harmonic rejection technique [12] is developed. The inputs of the HR-SSBmixer are 45°-spaced clocks generated by the divide-by-four circuit. The HR-SSBmixer effectively suppresses spurious tones resulted from the third- and fifth-order harmonics. As discussed in Section II-A,

TABLE II
FREQUENCY PLANNING

Standards	f_{min}~f_{max}(MHz)	Relation
WCDMA	2110~2117	$f_{vco}/2$
Bluetooth	2400~2483	$f_{vco}/2$
WLAN802.11a	5015~5850	$5f_{vco}/4$
WLAN802.11b	2400~2484	$f_{vco}/2$
WLAN802.11g	2400~2484	$f_{vco}/2$
TD-SCDMA	1880~1920 2010~2025 2300~2400	$f_{vco}/2$
DCS1800	1805~1880	$f_{vco}/2$

the LO phase noise requirement for the 802.11a mode is set by the integral noise. The spurious tone specification can thus be relaxed and this allows the 802.11a LO signal to be generated by the SSBmixer approach.

Table II summarizes the relations between the oscillator frequencies and the synthesizer output frequencies. The QVCO does not oscillate at the same frequency as that of the synthesizer output. As a result, the LO pulling is avoided. The synthesizer avoids the use of power-hungry high frequency LO path or broadband polyphase filters, and at the same time offers better spurious performance supporting major cellular and short-range wireless communication standards. Given the design being implemented in a 0.13-μm CMOS technology, the proposed synthesizer architecture and the frequency planning scheme offer a good tradeoff among synthesizer performance, hardware complexity and power efficiency.

III. CIRCUIT IMPLEMENTATION

A. QVCO With Phase Shifter

A QVCO consisting of two cross-coupled LC oscillator cores is adopted in designing the frequency synthesizer. The HR-SSBmixer uses the quadrature signals to carry out single sideband up-conversion and provides the LO signal for the 802.11a mode. Conventional cross-coupled quadrature oscillator has not been widely used because of its poor phase noise performance and potential bimodal oscillation. When two LC VCOs are coupled, the LC tanks operate away from the resonance frequency and thus the optimal quality factor (Q-factor) of the LC tanks is not reached [7]. As a result, the phase noise performance is degraded. Also the QVCO output frequency depends on the coupling strength of the two LC cores. Thus, there exists an additional flicker noise up-conversion mechanism due to the coupling transconductance and the cross-coupling transconductance modulation [13] leading to a $1/f^3$ phase noise degradation.

The issues mentioned above can be explained by the one-port model of a QVCO [14], as is shown in Fig. 2. At steady state, the

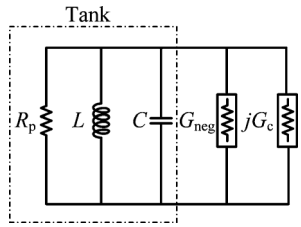

Fig. 2. A one-port model of the QVCO.

cross-coupling transistors produce a negative resistance $1/G_{\rm neg}$ canceling out the $R_{\rm p}$ while the coupling transistors produce a quadrature resistance $1/jG_c$ that acts on the LC tank and sets the frequency shift. The oscillation frequencies are calculated as

$$\omega_{\rm osc1,2} \approx \omega_0 \pm \frac{G_c}{2C} \tag{2}$$

where the $\pm$ signs are due to the output phase uncertainty of the two LC VCOs and ω_0 is the resonant frequency of the ideal LC tank. It can be seen from (2) that as the coupling strength increases, the oscillation frequency deviates from ω_0 by a larger amount. Since the tanks operate at a frequency that is different from the resonance frequency, the Q-factor is reduced deteriorating the QVCO phase noise. It is desirable to minimize the coupling strength to achieve a better phase noise. However, the mismatch between the two oscillators determines the minimum allowable coupling strength [15]. There exists a tradeoff between the phase noise and the output phase accuracy in the conventional transistor-coupled QVCO design.

Also can be seen from (2), there are two possible oscillation frequencies. Each output frequency corresponds to a lead or a lag phase relation between the outputs of the two VCOs [14]. In reality, asymmetric frequency response of the LC tanks due to the series inductive and capacitive losses results in a dominant mode which corresponds to a higher loop gain of the positive feedback in the oscillator [16]. However, the asymmetry introduced by the parasitic resistance does not guarantee a complete elimination of the unwanted oscillation. Various delays contributed by interconnect RC parasitics in the coupling path, and process and temperature variations may cancel the effect of the asymmetric frequency response of the LC tanks. Consequently, bimodal oscillation can still exist. This phenomenon is experimentally observed in [8]. Since the outputs of the QVCO serve as the inputs of the HR-SSBmixer, the phase relation of the quadrature outputs should be clearly defined in order to carry out a correct single sideband up-conversion operation.

To solve the problems mentioned above, a phase shifter can be used. The quadratrue output phases are still ensured by the coupling transistors, but the coupling currents are phase-shifted by 90°. This can be seen from the one port model in Fig. 2. If jG_c is multiplied by j, then it becomes part of the negative resistance and will not disturb the ideal LC tank. In fact, it will strengthen the negative resistance and improve the power efficiency. In addition, the phase-shift in the coupling path moves the QVCO operation away from the unstable boundary and effectively eliminates the bimodal oscillation [8]. Thus, introducing a phase shifter greatly decouples phase accuracy and phase noise performance, as it de-sensitizes the QVCO

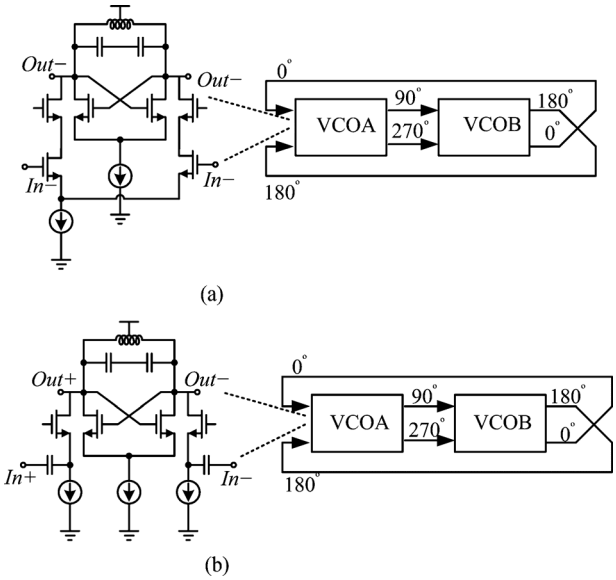

Fig. 3. (a) Phase shifter using cascode coupling stage. (b) Phase shifter using common gate coupling stage.

output phase error to the mismatches of the tail current and the tank Q-factor [15].

Introducing a phase-shift into the coupling path has been previously used to improve QVCO phase noise [7] and to avoid bimodal oscillation [8]. In Fig. 3(a), the coupling stage is constructed by a differential cascaded common-source common-gate configuration [8]. The cascode configuration creates a phase delay and moves the QVCO operation away from the unstable boundary, which eliminates the bimodal oscillation. However, the phase-shift from the cascode stage is limited to about 20°. It is enough to avoid the bimodal oscillation, but the phase noise improvement is limited. In addition, the noise from the cascode transistors is not negligible at high frequencies because of the parasitic capacitances. In Fig. 3(b), the $1/\mathrm{g_m}$ of the coupling transistor and the coupling capacitor are combined as a high-pass filter to introduce the phase-shift [7]. However, the Q-factor of the LC tank can be severely degraded due to the $1/\mathrm{g_m}$ input resistance of the coupling transistors.

In this paper, we propose a new phase shifter design as shown in Fig. 4. It is similar to the capacitive degeneration technique used in broadband amplifiers [17]. The tail current source of the coupling stage is first split and then a parallel R-C network between the source terminals of the coupling transistors is added. The resistors in the phase shifter consume no dc voltage drop which is appropriate for low-voltage applications. Since the R-C degeneration is not directly connected to the LC-tank, the Q-factor of the tank thus is not affected. The transconductance of the coupling stage is calculated as

$$G_{\mathrm{mc}} = \frac{g_{\mathrm{mc}}}{1+g_{\mathrm{mc}}R_{\mathrm{s}}} \cdot \frac{1+sR_{\mathrm{s}}C_{\mathrm{s}}}{1+\dfrac{sR_{\mathrm{s}}C_{\mathrm{s}}}{(1+g_{\mathrm{mc}}R_{\mathrm{s}})}} \tag{3}$$

where g_{mc} is the transconductance of the coupling transistor, and R_{s} and C_{s} are the resistance and capacitance in the phase-shift network. The transconductance has one zero and one pole. The zero frequency is $\omega_{\mathrm{z}} = 1/R_{\mathrm{s}}C_{\mathrm{s}}$ and the pole frequency is $\omega_{\mathrm{p}} \approx g_{\mathrm{mc}}/C_{\mathrm{s}}$. The zero results in a phase-lead to the transconductance while the pole results in a phase-lag. The total phase-shift thus can be derived as

$$\phi \approx \arctan\left(\omega R_{\mathrm{s}}C_{\mathrm{s}}\right) - \arctan\left(\frac{\omega C_{\mathrm{s}}}{g_{\mathrm{mc}}}\right). \tag{4}$$

Ideally, the shifted phase needs to be 90° at the operating frequency to align the current and the voltage of the tank. This requires that (5) is satisfied:

$$\frac{10}{R_{\mathrm{s}}C_{\mathrm{s}}} \le \omega_{\mathrm{osc}} \le \frac{g_{\mathrm{mc}}}{10C_{\mathrm{s}}}. \tag{5}$$

Equation (5) requires that the pole frequency is much larger than the zero frequency to have a 90° phase-shift. From (3), the magnitude of the coupling stage transconductance G_{mc} is source degenerated by R_{s}. If $g_{\mathrm{mc}}R_{\mathrm{s}}$ is too large, the resistive degeneration will result in a very small coupling transconductance at the resonance frequency and this may cause the phase accuracy of the QVCO to be degraded. Theoretically, if the coupling current is phase-shifted by 90°, then the bias current mismatch and the Q-factor mismatch between the two LC VCO cells will have no effect on the phase accuracy of the output signals. However, the phase accuracy can still be sensitive to the resonant frequency mismatch between the two tanks and the mismatch due to the two phase shifters [15]. Therefore, practically, the coupling strength cannot be too small even with the phase shifters adopted. A phase-shift of 50° is strong enough to increase the effective tank Q-factor and to improve the QVCO phase noise performance [15]. Therefore, considering the tradeoff between the phase noise and the phase accuracy, the phase shifter in the QVCO is designed to have a 40° $\sim$ 50° phase-shift at the operating frequency. It should be mentioned that R_{s} will introduce additional noise, but compared to the phase noise improvement due to the phase shifter, the noise degradation due to R_{s} can be neglected. Simulation also indicates that the noise contribution of R_{s} is negligible. It should be also noted that the discussions above are based on small-signal analysis. In actual design, the effective large-signal transconductance should be used. The small-signal analysis nevertheless provides a good explanation about the operating principle of the proposed phase shifter.

In this design, the QVCO operating frequency is from 3.6 to 5 GHz. The width of the coupling transistor is set as one half of that of the cross-coupling transistor. The coupling coefficient m is defined as $G_{\mathrm{mc,LS}}/G_{\mathrm{m,LS}}$, where $G_{\mathrm{mc,LS}}$ is the effective large-signal transconductance of the coupling stage and $G_{\mathrm{m,LS}}$ is the effective large-signal transconductance of the cross-coupling transistor. Due to the resistor degeneration, m is less than 1/2. Periodic steady-state (PSS) simulations show that m is 0.28 and the phase of the coupling current is shifted by 40° $\sim$ 50° at the operating frequency. The proposed phase shifter significantly improves the QVCO performance; this is verified by simulations. Simulation results of the QVCO with the proposed phase shifter scheme are compared with those of two circuits shown in Fig. 5. The first circuit is a conventional QVCO while the other is two LC oscillators coupled in an "in-phase" style. It has been proved that the in-phase coupled VCOs operate at the tank resonance frequency, and the phase noise performance is

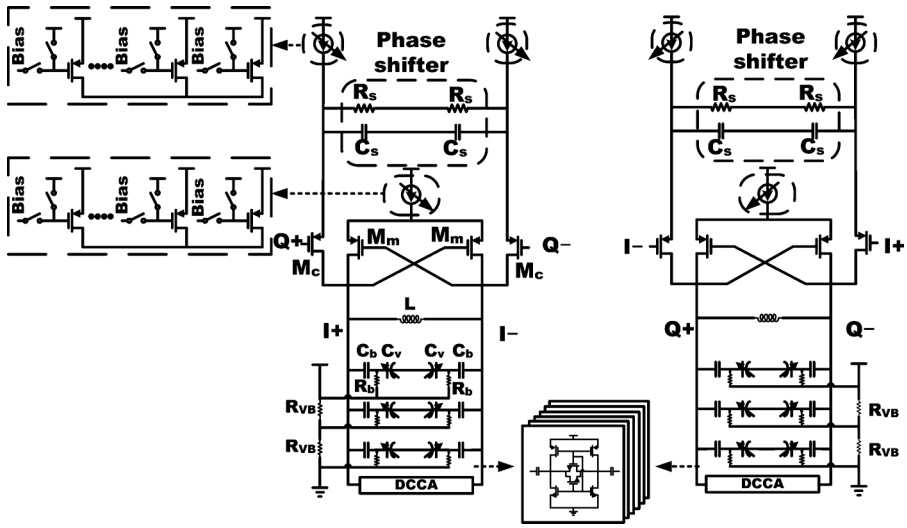

Fig. 4. QVCO with the proposed phase shifter.

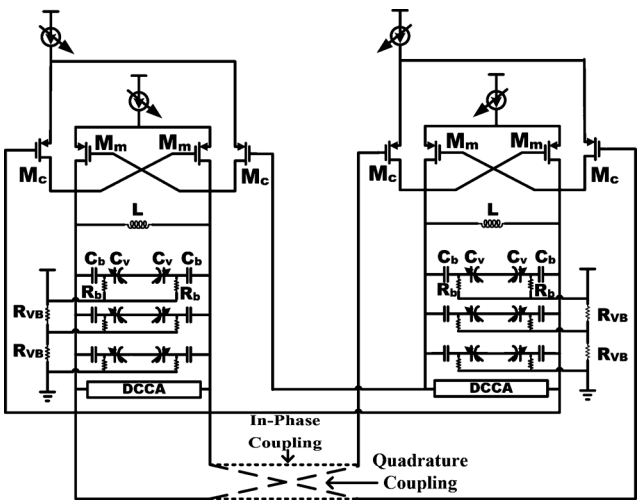

Fig. 5. Two oscillators coupled to operate in quadrature and in phase.

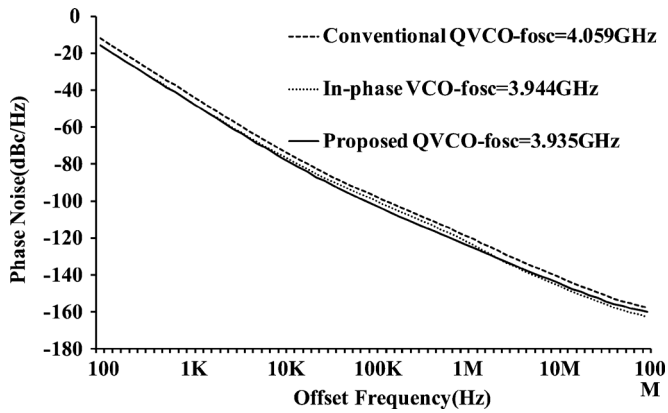

Fig. 6. Comparison of the phase noise simulation results.

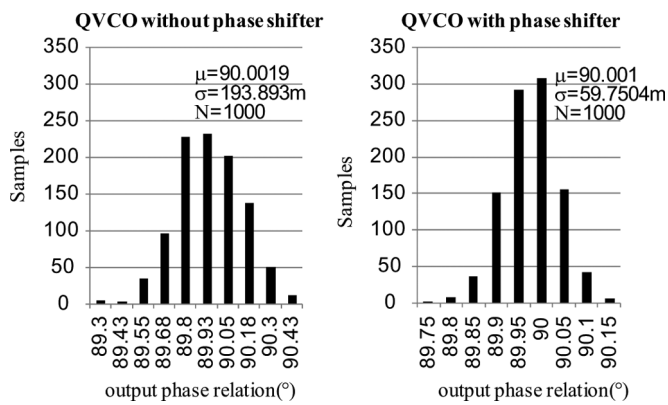

Fig. 7. Comparison of the output phase accuracy.

improved compared to a single VCO [18]. The transistor sizes, bias currents and LC tanks are all identical in these three circuits. Fig. 6 shows the phase noise comparison result. With the proposed phase shifter, the phase noise is improved by about 3 dB compared to the conventional QVCO. At some frequency points, the phase noise is even better than the LC-VCOs coupled in the "in-phase" style. It is also observed that the proposed QVCO operates at a frequency much closer to the LC tank resonance frequency while the conventional QVCO operates at a frequency which is 115 MHz apart from the ideal LC tank resonant frequency. This indicates the proposed QVCO has a larger effective Q-factor. Fig. 7 shows Monte Carlo simulation results. A coupling factor of 0.5 is assumed for the conventional QVCO which is larger than that of the proposed QVCO. Yet, the standard deviation of the output phase of the proposed QVCO is less than that of the conventional QVCO, which indicates that the proposed QVCO has a much better output phase accuracy.

B. HR-SSBmixer

As mentioned in Section II, by combining harmonic rejection and single sideband mixing, the HR-SSBmixer is developed to generate the 5 to 6 GHz LO frequency and avoid the use of broadband polyphase filters. The HR-SSBmixer carries out

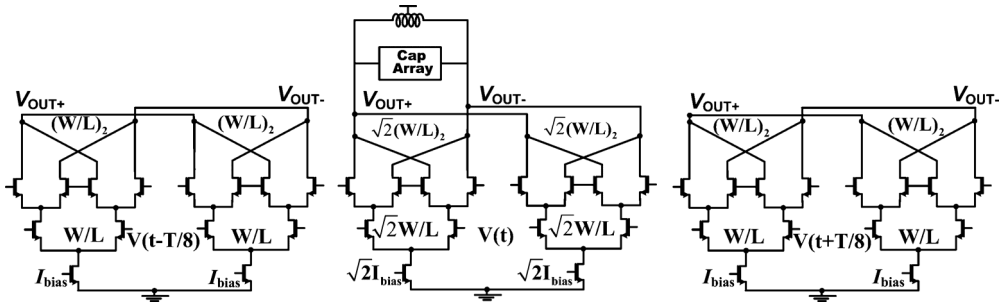

Fig. 8. Harmonic rejection SSBmixer.

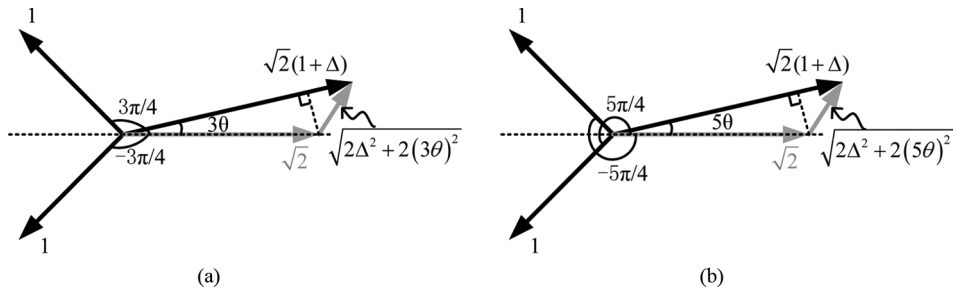

Fig. 9. Residual harmonics due to phase and gain mismatches: (a) third-order harmonic, and (b) fifth-order harmonic.

single sideband up-conversion to produce a $5 \times f_{\rm vco}/4$ LO frequency supporting the 802.11a standard and no filter is needed to reject the unwanted sidebands. The concept of harmonic rejection is firstly proposed in [12], which focuses on canceling harmonic components of a square-wave. It has also been used to solve the problem of harmonic mixing in the VHF and UHF TV bands [19]. The HR-SSBmixer, which is shown in Fig. 8, requires 8-phase inputs which are inherently generated by the divide-by-4 circuit following the QVCO as shown in Fig. 1. It is constructed by three SSB sub-mixers. Currents with different phases from the three SSB sub-mixers are summed at the common load to generate the output voltage, and the third- and fifth-order harmonics of $V(t)$ are canceled. A band-pass load which consists of an inductor and a 3-bit binary-coded capacitor array is used to reduce the power consumption and to suppress the residual spurious signals. It should be noted that two HR-SSBmixers are needed to generate the I/Q LO signals.

According to the time-shifting property of the Fourier Transform, for a periodical signal $x(t)$ with T being its period, the spectrum of $x(t - T/8)$ is $e^{-j\omega T/8}X(\omega)$. The phase-shift of the fundamental component is $\omega T/8 = \pi/4$. For the third- and fifth-order harmonics, the phase-shifts are $3\pi/4$ and $5\pi/4$, respectively. The phase-shifts of these three tones are different and this property can be used to linearize the SSBmixer's input signal, which is often a square-wave. By a summation of the signal $x(t)$ scaled by a factor of $\sqrt{2}$ and two time-shifted signals $x(t \pm T/8)$ having $\pm\pi/4$ phase-shifts relative to $x(t)$, the resulting signal eliminates the third and fifth harmonics while strengthens the fundamental component. In the single sideband conversion, quadrature signal of $x(t)$ is needed. The multi-phase signals are generated by the divide-by-4 circuit.

As the cancellation is performed in the current domain, the amplitude scaling of $\sqrt{2}$ is implemented by scaling the gain of the transconductance stage of the corresponding sub-mixer.

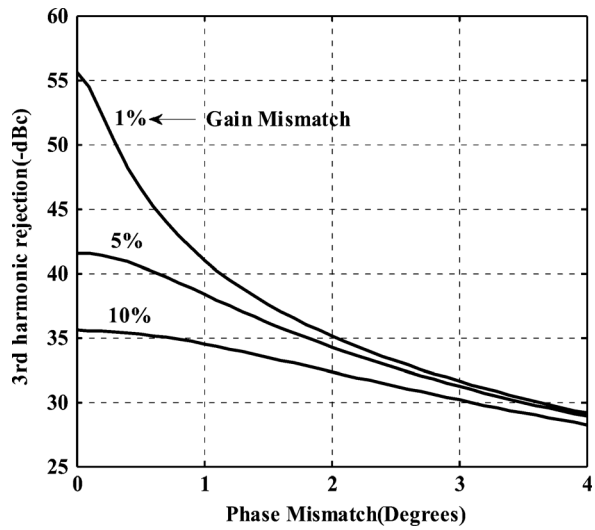

Fig. 10. Third-order harmonic rejection with respect to gain and phase mismatches.

Hence, for the circuit in Fig. 8, the harmonic rejection ratio highly depends on the phase matching of the input signals and the gain matching of the SSB sub-mixers [12]. Fig. 9 shows the phasor diagrams which illustrate the incomplete third- and fifth-order harmonic cancellations due to the gain and phase mismatches. Using the phasor diagrams, we derive the third- and fifth-order harmonic rejections as

$$\mathrm{HRM}_3 \approx \frac{1}{9}\frac{[2\Delta^2 + 2(3\theta)^2]}{\left(2\sqrt{2}\right)^2} \tag{6}$$

$$\mathrm{HRM}_5 \approx \frac{1}{25}\frac{2\Delta^2 + 2\,(5\theta)^2}{\left(2\sqrt{2}\right)^2} \tag{7}$$

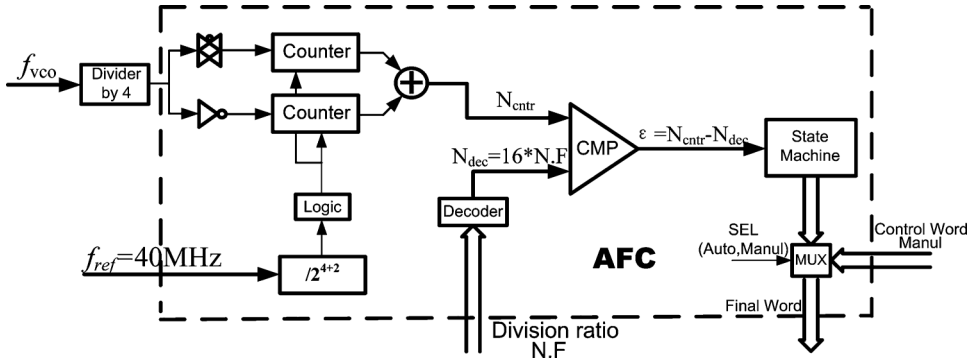

Fig. 11. AFC for coarse frequency tuning.

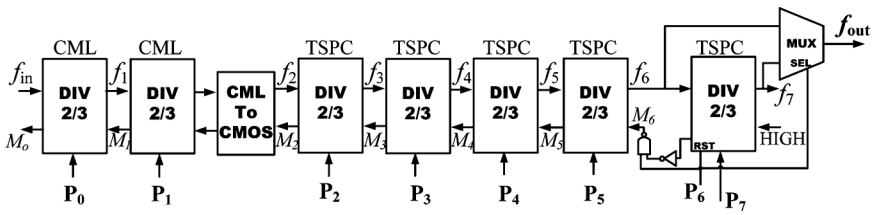

Fig. 12. Modular programmable divider.

where Δ is the gain mismatch and θ is the phase mismatch. The approximation holds for $\Delta \ll 1$ and $\theta \ll 1$ rad.

The input frequencies of the HR-SSBmixer are $f_{\rm vco}$ and $f_{\rm vco}/4$. Harmonic rejection is applied to the input whose frequency is $f_{\rm vco}/4$. The third- and fifth-order harmonics of this input will result in spurious signals at $f_{\rm vco} - 3f_{\rm vco}/4 = f_{\rm vco}/4$ and $f_{\rm vco} + 5f_{\rm vco}/4 = 9f_{\rm vco}/4$ due to the incomplete harmonic cancellations. The effect of the fifth-order harmonic can be neglected since $9f_{\rm vco}/4$ is far away from the supported frequency bands and any interference signals at that frequency can be suppressed by the receiver pre-filter. On the other hand, the interferences below 6 GHz may not be attenuated by the receiver front-end pre-filter, thus the spurious signals due to the third-order harmonic needs to be minimized. Using (6), the $\rm HRM_3$ with respect to the phase and gain mismatches is plotted in Fig. 10. As can be seen from the figure, a better than 40 dB third-order harmonic rejection requires a less than 1% gain mismatch and a less than 1° phase mismatch.

The requirements of the third-order harmonic rejection and the sideband rejection for the HR-SSBmixer are determined by the frequencies of the spurious signals and the possible interferences. In the design, the output frequency of the HR-SSBmixer is from 5.15 to 5.85 GHz. Therefore, the frequency of the image sidebands is from 3.09 to 3.51 GHz, and the third-order harmonic frequency is from 1.03 to 1.17 GHz. The third-order harmonic does not fall into any major wireless communication standards. When the receiver operates in the 802.11a U-NII upper band (5.725 $\sim$ 5.825 GHz), the WiMax signal whose frequency is from 3.3 to 3.8 GHz could interfere with the receiver operation since the image sideband of the HR-SSBmixer is from 3.435 to 3.495 GHz. The 802.11a U-NII lower- and middle-band (5.15 $\sim$ 5.35 GHz) operations with an image sideband from 3.09 to 3.21 GHz will not be affected by the WiMax signal. The required image sideband rejection ratio of the HR-SSBmixer is thus set by the WiMax signal interference and possibly the amount of interference suppression from the receiver front-end pre-filter.

C. Other Circuit Blocks

In order to increase the QVCO tuning range and reduce the QVCO gain, a switched capacitor bank is used in the resonator. An automatic frequency calibration technique is adopted in the synthesizer to ensure that a proper tuning curve of the QVCO can be selected. The detailed implementation of the AFC is shown by Fig. 11. The QVCO output signal is divided by 4 to lower the input frequency of the AFC. The divide-by-4 circuit reuses the first two stages of the programmable divider to save area and power. Differential signals are used for frequency detection to improve the counting accuracy. In generating the differential signals, a transmission gate is inserted to compensate the inverter delay. An AFC and QVCO co-design scheme is also developed to ensure a correct PLL locking.

The programmable divider in this fractional-N frequency synthesizer is shown in Fig. 12. It is based on a modular architecture described in [20]. A total of seven stages of div2/3 cells are cascaded with one division ratio extension cell. The first two stages are implemented using CML logic circuits. The programmable divider is dynamically controlled by the sigma-delta modulator. The sigma-delta modulator, on the other hand, is clocked by the output of the programmable divider. Thus, it is important to ensure that the control bits of the programmable divider are updated at the right time [21]. Fig. 13 shows the timing diagram of the fractional-N PLL. $f_{\rm out}$ is the output of the programmable divider. The sigma-delta modulator is triggered by the falling edge of $f_{\rm out}$ and the control bits of the programmable divider are updated by the rising edge of $f_{\rm out}$. With this arrangement, the division ratio is safely updated at every reference cycle without interfering with

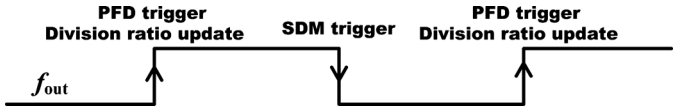

Fig. 13. Timing diagram of the fractional-N PLL.

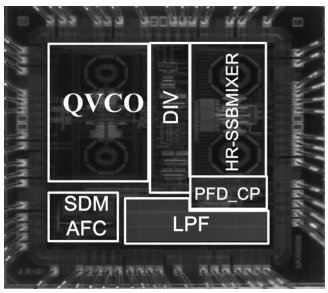

Fig. 14. Die microphotograph.

the operation of the programmable divider. In addition, the divider swaps between a 6-cell mode and a 7-cell mode when the division ratio is between 124 and 129. Since the output of the divider needs to have no phase hopping to ensure a proper sigma-delta control [2], a multiplexer dynamically chooses f_6 or f_7 as the divider output. Reset (*RST*) of the seventh div2/3 cell ensures its output will stay at zero when it is disabled.

IV. Measurement Results

The wideband multi-standard frequency synthesizer is implemented in a TSMC 0.13-μm CMOS technology, with all the circuit blocks integrated on chip. A die microphotograph of the chip is shown in Fig. 14. The chip area is 1.86 mm $\times$ 1.8 mm with an active core area of 1.86 mm^2.

The bandwidth of the PLL ranges from 60 to 90 kHz. The reference frequency is 40 MHz. All circuit blocks are powered by a 1.2 V supply. Power consumption is measured for different standards. For the 802.11a mode, the HR-SSBmixer is turned on and the total power consumption ranges from 49.12 to 52.62 mW. For other supported standards, the power consumption is from 35.6 to 44 mW. The measurement results of the frequency synthesizer are summarized in Table III. The performance of the proposed QVCO is measured with a fixed control voltage. The output spectrum is measured by an Agilent E4440A spectrum analyzer. The frequency tuning curves are shown in Fig. 15. The measured QVCO gain is 25 MHz/V to 105 MHz/V. As shown in Fig. 4, the varactors with three different DC biasing voltages are connected in parallel to achieve more linear tuning curves. The measured VCO tuning curves in Fig. 15 validate the linearization technique. The FOM of the QVCO, as defined in [13], is from 179.5 to 185.2 dB with power consumptions ranging from 7.68 to 17.76 mW. As shown in Table IV, except for this work, the oscillators in other publications are all non-quadrature VCOs. The FOM of the proposed QVCO is comparable to those of the single LC-VCOs. To validate the simulation results shown in Section III-A, the simulated and measured QVCO phase noises are compared. The phase noise is measured by an Agilent E5052B signal source analyzer. The simulated and measured QVCO phase noises at a frequency of 4.09 GHz are shown in Fig. 16 and they agree very well with each other.

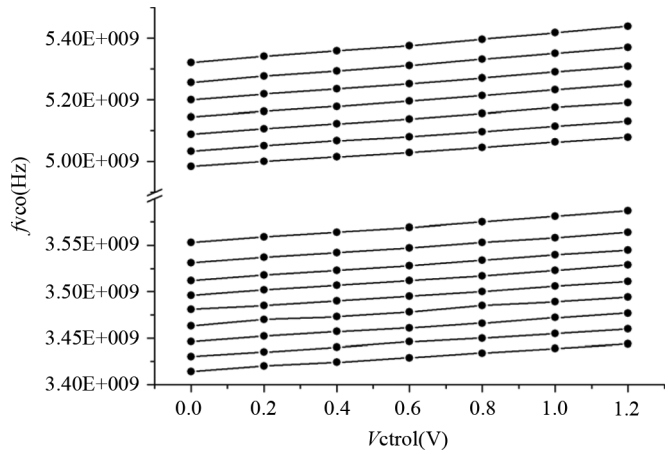

Fig. 15. Measured tuning curves of the QVCO.

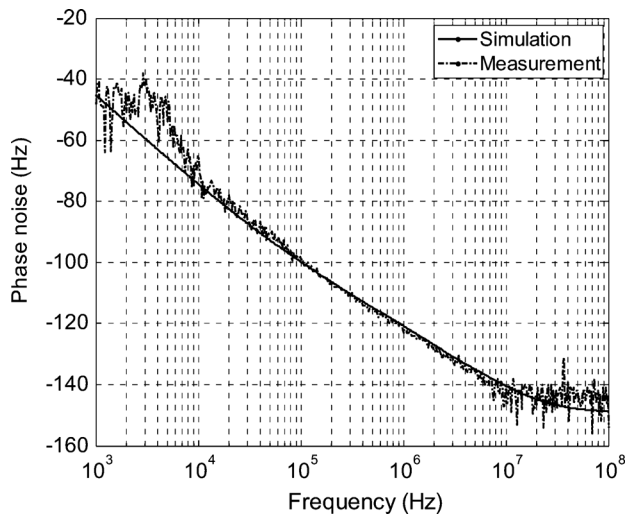

Fig. 16. Comparison between simulated and measured QVCO phase noise at 4.09 GHz.

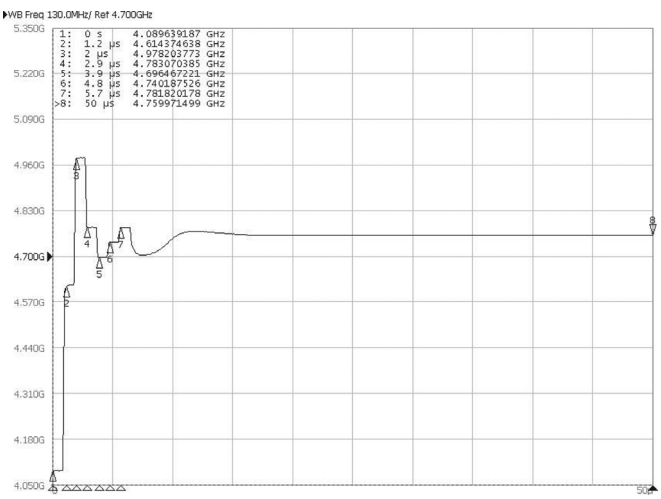

Fig. 17. Measured PLL settling time.

The overall locking time of the frequency synthesizer is the sum of the AFC time and the PLL settling time. The locking process of the PLL is measured by an Agilent E5052B signal source analyzer. Fig. 17 shows the transient response at the

TABLE III
SUMMARY OF THE MEASUREMENT RESULTS

Standards	Measured phase noise		Simulated phase noise	Phase noise design target
	Spot phase noise	RMS phase noise		
DCS1800 (1805~1880MHz)	-119.6 dBc/Hz@600 kHz -130.4 dBc/Hz@1.6 MHz -136.1 dBc/Hz@3 MHz	0.64°	-119.5 dBc/Hz@600 kHz -130.2 dBc/Hz@1.6 MHz -136.2 dBc/Hz@3 MHz	-119 dBc@600 kHz -129 dBc@1.6 MHz -136 dBc@3 MHz
WCDMA (2110~2170MHz)	-92.2 dBc/Hz@100 kHz -121.5 dBc/Hz@1 MHz -150 dBc/Hz@100 MHz	0.89°	-95 dBc/Hz@100 kHz -122.5 dBc/Hz@1 MHz -160 dBc/Hz@100 MHz	-108.8 dBc@7.6 MHz -120.8 dBc@15 MHz -150 dBc@130MHz
TD-SCDMA (1880~2400MHz)	-93.5 dBc/Hz@100 kHz -121.4 dBc/Hz@1 MHz -132.4 dBc/Hz@3.2 MHz	0.8°	-92.4 dBc/Hz@100 kHz -122.1 dBc/Hz@1 MHz -134 dBc/Hz@3.2 MHz	-111 dBc@3.2 MHz -123 dBc@5 MHz
Bluetooth/802.11b/g (2400~2480MHz)	-92 dBc/Hz@100 kHz -119.6 dBc/Hz@1 MHz -144.9dBc/Hz@20 MHz	0.95°	-91.6 dBc/Hz@100 kHz -120.1 dBc/Hz@1 MHz -149dBc/Hz@20 MHz	-81 dBc@1 MHz -111 dBc@2 MHz -121 dBc@3 MHz
802.11a (5180~5805MHz)	-85.2 dBc/Hz@100 kHz -115.2 dBc/Hz@1 MHz -141.5 dBc/Hz@20 MHz	1.8°	-85.2 dBc/Hz@100 kHz -115.2 dBc/Hz@1 MHz -142.5 dBc/Hz@20 MHz	-90 dBc@10 kHz -100.2 dBc@20 MHz -116.2 dBc@40 MHz
Loop bandwidth	60 kHz ~ 90 kHz			
Locking time	<50 μs (BW = 90 kHz)			
Reference Spur	<-69 dBc@40 MHz			
Fractional Spur	-72.93 dBc@1 MHz			
Power Dissipation mW	49.12~52.62(802.11a);35.6~44(standards except 802.11a)			
	QVCO: 7.68~17.8		HR-SSBmixer: 8.35	
	QVCO Buffer: 11~12.7		Divide-by-2(incl. buffer): 4.58	
	PLL (without osc.): 11.08		Divide-by-4(incl. buffer): 8.11	
Die Area	$1.36\times1.37\ \text{mm}^2$ (core circuits)			

QVCO output when the PLL is in the locking process. The clock frequency of the AFC is 40 MHz. It takes 8 cycles for the AFC to complete the tuning curve searching. Each cycle contains 32 AFC clock periods. The first 7 cycles are used for AFC counting and the last cycle is used to determine the correct tuning curve which is the closest to the target frequency. Therefore, the theoretical AFC search time is about 6.4 μs which is validated by the measurement result. The overall locking time is less than 50 μs.

The synthesizer phase noise measurement is carried out by an Agilent E5052B signal source analyzer. Fig. 18 shows the measured phase noises. The in-band phase noise of the 1.87 GHz LO corresponding to the DCS 1800 standard is -92 dBc/Hz. The spot phase noises are -119.6, -130.4, and -136 dBc/Hz at 600 kHz, 1.6 MHz and 3 MHz frequency offset, respectively, satisfying the design specifications. Measurement results show that a -121.58 dBc/Hz phase noise at 1 MHz offset frequency is achieved at 2.17 GHz which is in the WCDMA frequency band. As mentioned in the system design section, the far-out phase noise is also important for the WCDMA mode. The phase noise measurement shows that the noise floor is -150 dBc/Hz, which satisfies the requirement. There exists a ~ 10 dB difference between the simulated and measured noise floors. The deteriora-

TABLE IV
MULTI-STANDARD ANALOG FREQUENCY SYNTHESIZER PERFORMANCE COMPARISON

	[1]	[24]	[5] [A]	[2]	This work
Technology	0.25-μm BiCMOS	0.13-μm CMOS	0.13-μm CMOS	45-nm CMOS	0.13-μm CMOS
Power(mW)	NA	40.8~69.6	5.28~28.8 [A]	21.45~31.35[B]	35.60~52.62
Area(mm^2)	1.7×1.5	NA	NA	1.02×0.4	1.36×1.37
Output Range(GHz)	0.8~5.8	0.1~6	0.1~6	0.1~5	1.8~6
Phase Noise @1 MHz	-123 dBc/Hz (LO:3.77 GHz)	-115 dBc/Hz (LO:4 GHz)	-115dBc/Hz (LO:5 GHz)	-112 dBc/Hz (LO:7.2 GHz)	-115 dBc/Hz (LO:5.18 GHz)
VCO/QVCO *FOM*(dB)	189.25	178~188	179~185	183	179.5~185.2
AFC Integration	NO	NO	NO	NO	YES
Spur Performance(dBc)	NA	NA	<-30 @SSBmixer	NA	-69@40 MHz -72.93@1 MHz <-42.4@HR-SSBmixer

[A] Power consumption of the PLL is not included. Phase noise and VCO data are from [25].

[B] Power consumption of the LO generation circuits outside the PLL is not included.

tion is due to the test buffer. The simulated QVCO phase noises before and after the test buffer confirm the noise floor difference. For TD-SCDMA, Bluetooth and 802.11 b/g standards, the phase noise is from -118 to -121 dBc/Hz at 1 MHz and the in-band phase noise is about -90 dBc. For the 802.11a standard, the measured phase noise at 1 MHz offset frequency ranges from -113 to -115 dBc/Hz. However, the close-in phase noise is -85 dBc/Hz and the resulting RMS noise, which is integrated from 10 kHz to 100 MHz, is about 2°, or -29 dBc. This result does not meet our design target. This, however, can be corrected by reducing the charge pump noise. The RMS noises of other standards integrated from 1 kHz to 100 MHz are also shown in Fig. 18 and are less than 1°. The phase noise and the fractional spurs are degraded when the integer number of the division ratio is around 128. The reason is that the nonlinearity of the divider becomes important in this situation due to the divide-modulus-dependant delay. The programmable divider in Fig. 12 swaps between the 6-cell and 7-cell configurations and the delays from the input to the output of multiplexer are different in these two configurations. The nonlinearity of the divider degrades the SDM output pattern's randomness and folds the quantization noise back in-band. This problem can be solved by adding a retiming flip-flop at the output of the multiplexer.

The measured reference spur at 40 MHz as shown in Fig. 19 is about -70 dBc. Fig. 20 shows that the measured fractional spur at 1 MHz is -72.93 dBc. The reference spur at the 40 MHz offset frequency is important for the 802.11a/g modes. The measured reference spurs safely meet the design requirements listed in Table I. The measured in-band fractional spurs are from -33 dBc to -42 dBc. The in-band fractional spurs are worse than those measured at 1 MHz frequency offset since they are less attenuated by the PLL. The in-band fractional spurs can be further reduced by improving the charge pump linearity. Table III summarizes the measurement results mentioned above. It also includes the simulated phase noise results which are published in [6], and the design targets of the spot phase noise.

The output spectrum of the HR-SSBmixer is shown in Fig. 21. The markers 1, 2, and 3 indicate the suppression of the QVCO signal feedthrough from the HR-SSBmixer's input to its output, the image signal suppression and the third-order input harmonic suppression, respectively. The QVCO signal feedthrough can be further improved. However, since the QVCO does not oscillate at any of the frequency bands of the supported standards, the QVCO signal feedthrough itself is not a major issue. The results of the third-order harmonic rejection (HRM_3) and the image rejection ratio (IRR) are plotted in Fig. 22. The rejection ratios across the entire 802.11a frequency band are all greater than 40 dB. Simulations, however, find that the HRM_3 and the IRR in the same frequency band are over 50 dB and the QVCO signal feedthrough is less than -65 dBc. We believe that the QVCO signal leakage is due to the substrate leakage and the electric-magnetic coupling between the two inductors, which are not included in the post-layout simulations. The intermodulation between the QVCO leakage signal and the desired LO can deteriorate the HRM_3 and the IRR through the test buffer nonlinearity. As discussed in Section III-B, the image sideband of the HR-SSBmixer falls into the WiMax frequency band when the receiver operates in the 802.11a U-NII upper-band mode. The measured IRR is from 49.1 dBc to 57.1 dBc for this frequency band. The SNR specification for 802.11a is 28 dB [10]. Thus, the maximum allowed WiMax

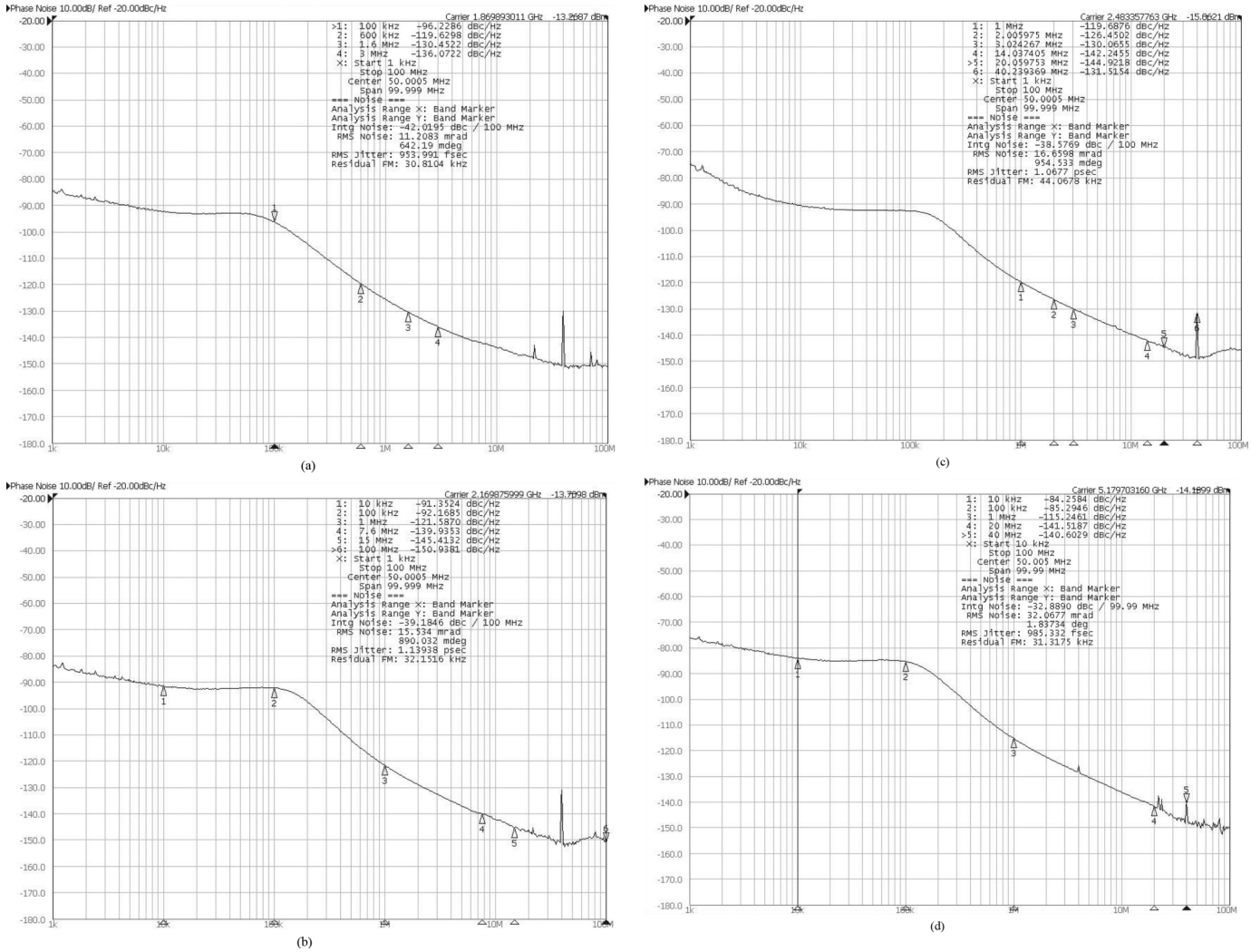

Fig. 18. Phase noise measurement results: (a) DCS1800, (b) WCDMA, (c) Bluetooth/ 802.11b/g, (d) 802.11a.

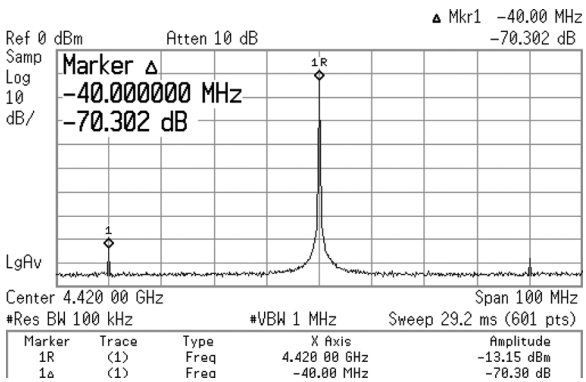

Fig. 19. Measured reference spurs.

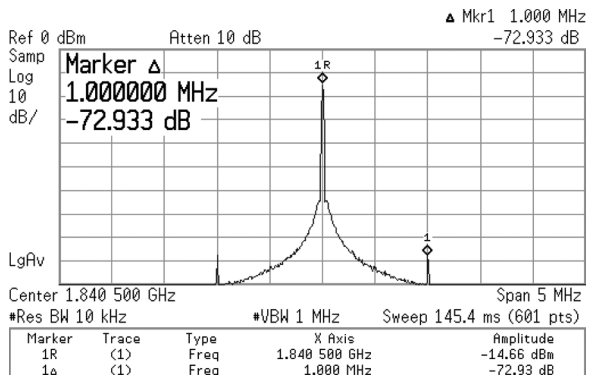

Fig. 20. Measured fractional spurs.

interference signal level is 21 ∼ 29 dB greater than the desired signal level assuming no suppression by the receiver front-end pre-filter. This number can be further improved to 52 dB by adding a calibration circuit to the HR-SSBmixer [22]. If the interference signal level is much stronger than the above numbers, then a dedicated SAW filter for the 802.11a mode is needed at the receiver front-end to further suppress the WiMax interference signal. To estimate the phase accuracy of the LO signals, the IRR of the SSBmixer of the transmitter can often be used [23]. However in our case, the IRR is affected by many factors. The I/Q amplitude/phase mismatches of the QVCO signals and the divide-by-4 output signals as well as the test buffer nonlinearity all can deteriorate the sideband rejection while the band-pass frequency response of the HR-SSBmixer's

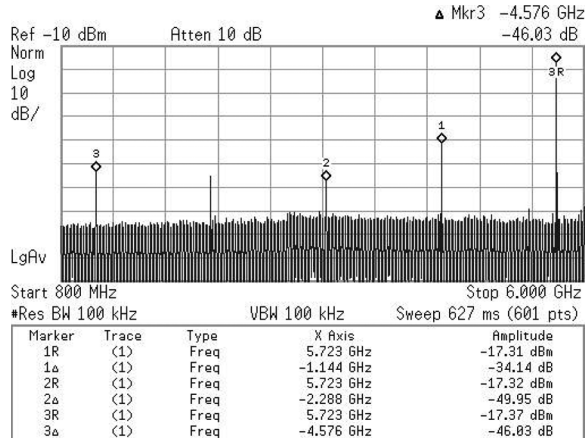

Fig. 21. HR-SSBmixer output spectrum.

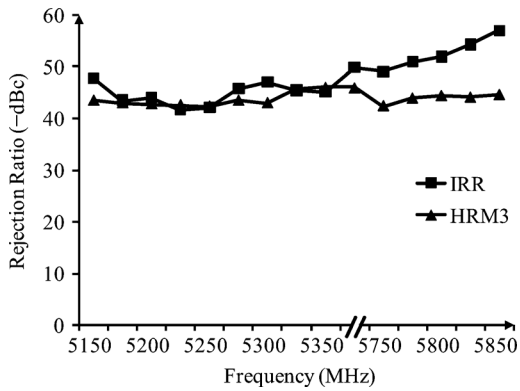

Fig. 22. Third-order harmonic rejection and image rejection of the HR-SSB-mixer.

load improves the rejection ratio to some extent. As a rough estimation, we assume that the QVCO phase mismatch mainly causes the image sideband. Since the sideband rejections shown in Fig. 22 are all larger than 41.7 dBc, the worst case QVCO output phase mismatch can thus be estimated to be 0.94° [23]. In Fig. 21 a spurious signal is found at $f_{\rm VCO}/2$ which falls into the WCDMA frequency band. It is due to the signal leakage from the divide-by-2 circuit's output to the output of the HR-SSBmixer. This can be solved by separating the power supplies of the divide-by-2 and the divide-by-4 circuits. The divide-by-2 circuit can then be turned off when the HR-SSBmixer is activated for generating the 802.11a carrier frequency. Table IV compares the proposed synthesizer design with recently published state-of-the-art multi-standard analog LO generation systems for wireless applications. In the comparison table, it should be mentioned that [2], [5], [24] use lookup tables instead of AFC to search the VCO tuning curves. The lookup table method, however, often requires extra on-chip process-voltage-temperature (PVT) detection circuits to update the table contents, while the AFC approach inherently counteracts the PVT variations.

V. Conclusion

A fractional-N frequency synthesizer for cellular and short-range wireless communication receiver is presented. The synthesizer supports the standards of DCS1800, WCDMA, TD-SCDMA, WLAN 802.11 a/b/g and Bluetooth. Architecture design and frequency planning are carefully performed to ensure that the synthesizer meets the specifications of the above mentioned standards and at the same time achieves an optimal tradeoff among synthesizer performance, hardware complexity and power efficiency. A new phase-shift scheme to improve QVCO phase noise and to eliminate bimodal oscillation is developed. Combining harmonic rejection and single sideband mixing, the HR-SSBmixer is developed to suppress spurious signals. The residual spurs due to phase and gain mismatches are analyzed. Designed in a 0.13-μm CMOS technology, the synthesizer occupies an active area of 1.86 mm^2 and consumes 35.6 to 52.62 mW of power. Measurement results show that the synthesizer frequency range, the phase noise, the settling time and the spur performances meet the design specifications of the standards mentioned above. It should be mentioned that the synthesizer performance also meets the WLAN and Bluetooth transmitter requirements. This is important since for WLAN and Bluetooth applications, often there is only one frequency synthesizer for both the transmitter and the receiver. The PLL close-in phase noise can be further improved in the 802.11a mode to reduce the RMS noise. This can be achieved by optimizing noise and linearity of the charge pump. A retiming circuit can be added to the programmable divider to ensure that its nonlinearity does not impair PLL in-band phase noise. The HR-SSBmixer spur rejection can be further increased by strengthening the isolation between the QVCO and the HR-SSBmixer.

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