On the reduced-complexity of LDPC decoders for ultra-high-speed optical transmission

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Abstract: We propose two reduced-complexity (RC) LDPC decoders, which can be used in combination with large-girth LDPC codes to enable ultra-high-speed serial optical transmission. We show that optimally attenuated RC min-sum sum algorithm performs only 0.46 dB (at BER of 10^{-9}) worse than conventional sum-product algorithm, while having lower storage memory requirements and much lower latency. We further study the use of RC LDPC decoding algorithms in multilevel coded modulation with coherent detection and show that with RC decoding algorithms we can achieve the net coding gain larger than 11 dB at BERs below 10^{-9}.

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References and links

1. Introduction

In response to high-bandwidth demands due to rapid growth of data-centric applications and deployment of broadband access networks, the network operators are upgrading their dense wavelength division multiplexing (DWDM) networks from 10Gb/s per channel to more spectrally efficient 40 Gb/s and 100 Gb/s [1]. The 40 Gb/s and 1 Tb/s serial optical transmissions are regarded to be the next steps after 100Gb/s and have already started attracting interests from research community in both academia and industry [2]. In order to achieve ultra-high-speed optical transmission at 400Gb/s and beyond with commercially available equipment operating at 40 Giga symbols/s (40 GS/s), we have recently proposed the use of iterative polarization quantization (IPQ)-based modulation scheme with component codes being large-girth low density parity check (LDPC) codes [3]. This scheme, however, requires the implementation of sum-product algorithm (SPA), commonly used in decoding of LDPC codes, at 40 Gb/s, which is challenging to implement even with state-of-the-art electronic integration circuits technology.

In order to reduce the complexity of SPA, a number of different approximate algorithms were proposed [2,4,5]. The main focus was to reduce the complexity of check-node (c-node) update rule. Because c-node update rule is the key step in SPA, imperfect approximations lead to significant BER performance degradation. In this paper we follow a different strategy. Instead of trying to reduce the complexity of c-node update rule, we try to reduce the complexity of variable-node (v-node) update rule. Two reduced complexity (RC) LDPC decoding algorithms are introduced: (i) RC min-sum algorithm and (ii) RC a posteriori
probability (APP) algorithm. We show that even complete elimination of v-node update rule leads to only 0.46 dB degradation when large-girth LDPC codes are used. We further study the use of RC decoding algorithm in polarization multiplexed (PolMUX) 32-IPQ with symbol rate of 50 Giga symbols/s (50 GS/s) and show that that net coding gains (NCGs) beyond 11 dB (at BER \( \leq 10^{-7} \)) are possible.

The paper is organized as follows. In Section 2, we provide two RC LDPC decoding algorithms and evaluate their BER performance, decoding complexity, and memory requirements. In Section 3, we describe polarization-multiplexed IPQ scheme suitable for ultra-high-speed serial optical transmission and evaluate its performance when the proposed RC LDPC decoding algorithms are used. Concluding remarks are given in Section 4.

2. Reduced-complexity LDPC decoders

Before we fully describe the proposed RC algorithms, we introduce several definitions that will facilitate the description. A regular \((n, k)\) LDPC code is a linear block code whose parity-check matrix \(H\) contains exactly \(Wc\) 1’s per column and exactly \(Wr\) = \(Wc \times (n-k)\) 1’s per row, where \(Wc < k\). Decoding of LDPC codes is based on SPA, which is an iterative decoding algorithm where extrinsic probabilities are iterated forward and back between variable and check nodes of bipartite (Tanner) graph representation of a parity-check matrix \(H\). The Tanner graph of an LDPC code is drawn according to the following rule: check node \(c\) is connected to variable node \(v\) whenever element \(h_{cv}\) in \(H\) is a 1. For v-node \(v\) (c-node \(c\)) we define its neighborhood \(N(v) (N(c))\) as the set of c-nodes (v-nodes) connected to it. For the completeness of presentation we briefly describe the log-domain SPA (for detailed description an interested reader is referred to [2]).

Gallager SPA

0. Initialization: For \(v = 0,1,\ldots,n-1\); initialize the messages \(L_{c\rightarrow v}\) to be sent from v-node \(v\) to c-node \(c\) to channel log-likelihood ratios (LLRs) \(L_{ch}(v)\), namely \(L_{v\rightarrow c} = L_{ch}(v)\).

1. c-node update rule: For \(c = 0,1,\ldots,n-1\); compute \(L_{c\rightarrow v} = \sum_{N(c)\ni v} L_{v\rightarrow c}\). The box-plus operator is defined iteratively by

\[
L_{c} = \prod_{x=1}^{2} \text{sign}(L_{x}) \cdot \phi \left( \sum_{x=1}^{N} \phi(L_{x}) \right), \quad \phi(x) = -\log(\tanh(x/2)).
\]

The box operator for \([N(c)\ni v]\) components is obtained by recursively applying 2-component version defined above.

2. v-node update rule: For \(v = 0,1,\ldots,n-1\); set \(L_{v\rightarrow c} = L_{ch}(v) + \sum_{N(v)\ni c} L_{c\rightarrow v}\) for all c-nodes for which \(h_{cv} = 1\).

3. Bit decisions: Update \(L(v) (v = 0,\ldots,n-1)\) by \(L(v) = L_{ch}(v) + \sum_{N(v)\ni c} L_{c\rightarrow v}\) and set \(\hat{v} = 1\) when \(L(v) < 0\) (otherwise, \(\hat{v} = 0\)). If \(\hat{v}H = \mathbf{0}\) or pre-determined number of iterations has been reached then stop, otherwise go to step 1.

*The channel LLR is defined by \(L_{ch}(v) = \log(P(v = 0|y)/P(v = 1|y))\), where \(y\) is the channel sample. For example, for asymmetric AWGN channel \(L_{ch}(v) = \log(\sigma_{1}/\sigma_{0}) \cdot (y-\mu_{0})^{2}/2\sigma_{0}^{2}\) + \((y-\mu_{1})^{2}/2\sigma_{1}^{2}\), while for symmetric AWGN \((\sigma_{1} = \sigma_{0} = \sigma)\) channel \(L_{ch}(v) = 2y/\sigma^{2}\), where \(\mu_{i}, (\sigma_{i})\) denote the mean (standard deviation) corresponding to symbol \(i (i = 0,1)\).

Because the c-node update rule involves log and tanh functions, it is computationally intensive, and there exist many approximation approaches. A popular one is the min-sum-plus-correction-term approximation [4]. Namely, it can be shown that “box-plus” operator \(\boxplus\) can also be calculated by \(L_{c} = \prod_{x=1}^{2} \text{sign}(L_{x}) \cdot \min(L_{x}, L_{y}) + c(x,y)\), where \(c(x,y)\) denotes the correction factor defined by \(c(x,y) = \log(1 + \exp(-|x + y|)) - \log(1 + \exp(-|x-y|))\), commonly
implemented as a look-up table (LUT). In our approach, we concentrate on variable node update rule in order to reduce the complexity of SPA. It is clear from algorithm above that the computational complexity of c-node update rule is much higher than that of v-node, while memory storage requirements are comparable. Because the v-node update rule step is not that critical compared to c-node update rule, we propose to completely eliminate it. Our reduced complexity SPA, which will be called here RC-min-sum algorithm given below, is therefore composed only steps 1 and 3. To compensate for BER performance loss due to elimination of v-node update rule we propose to re-formulate the c-node update rule by introducing the attenuation factor $\alpha$ in box-plus operator as follows: $L_{c,v} \equiv \alpha \sum_{k} \text{sign}(L_k) \min(|L_k|,|L_0|)$. In addition to reducing memory storage requirements, the proposed RC algorithm improves the latency, which is of crucial importance for ultrahigh-speed implementation. The RC min-sum algorithm can be formulated as follows.

Reduced-complexity min-sum algorithm

0. Initialization: For $v = 0,1,\ldots,n-1$; initialize the v-node reliabilities $L_v$ to channel LLRs, $L_v = L_{c,v}(v)$.

1. c-node update rule: For $c = 0,1,\ldots,n-k-1$; compute $L_{c,v} = \sum_{k} L_k$. The box-plus operator is defined by $L_{c,v} \equiv \alpha \sum_{k} \text{sign}(L_k) \min(|L_k|,|L_0|)$.

2. Bit decisions: Update $L(v)$ ($v = 0,\ldots,n-1$) by $L(v) = L_c(v) + \sum_{k} L_{c,v}$ and set $\hat{v} = 1$ when $L(v) < 0$ (otherwise, $\hat{v} = 0$). If $\hat{v}H^T = 0$ or pre-determined number of iterations has been reached then stop, otherwise go to step 1.

The second RC algorithm to be described here is based on the RC decoding algorithm proposed by Fossorier et al. [5]. The original algorithm was applicable to AWGN channels only. Our proposed algorithm, which will be called here reduced complexity a posteriori probability (RC-APP) algorithm, is independent on channel assumption and can be formulated as follows.

Reduced complexity a posteriori probability algorithm

0. Initialization: For $v = 0,1,\ldots,n-1$; determine hard decisions $z_v = \{1-\text{sign}[L_{c,v}(v)]\}/2$ and magnitudes $m_v = |L_{c,v}(v)|$ from channel LLRs $L_{c,v}(v)$.

1. c-node update rule: For $c = 0,1,\ldots,n-k-1$; compute the magnitudes $m_{c,v}$ to be sent from c-node $c$ to v-node $v$ by $m_{c,v} = \alpha \min m_i$. where $\alpha$ is the attenuation factor. Compute also $z_{c,v} = \left(\sum_{k} z_k\right) \mod 2$.

2. Bit decisions: Update the v-node magnitudes $m_v$ ($v = 0,\ldots,n-1$) by $m_v = |L_{c,v}(v)| + \sum_{k} (1-2z_{c,v}) m_{c,v}$ and set $z_v = z_v \oplus 1$ for $m_v < 0$. If $\hat{v}H^T = 0$ or pre-determined number of iterations has been reached then stop; otherwise go to step 1.

Note that this algorithm requires only the use of summations, comparators and mod 2 adders. The attenuations can be implemented by appropriate register shifts (e.g., 0.5 corresponds to one register shift to the right). The decoding complexity can be estimated in terms of number of required operations per single iteration. For example, the c-node update rule in RC-min-sum algorithm is dominated by number of comparators, which is $(d_c-2)$, where $d_c$ is the c-node degree. The conventional min-sum algorithm requires $d_c$-additions (where $d_c$ is the v-node degree) in v-node update rule, while the bit-decision step requires $(d_c + 1)$ additions. Therefore, the RC-min-sum algorithm requires $nd_c$ additions less compared to
conventional min-sum algorithm. The complexity of Gallager SPA is even higher since the c-node update rule requires $15(d_r-2)$ additions per check node. To study the memory allocation requirements, we assume that partially parallel implementation is used, with bit-processing elements (BPEs) and check processing elements (CPEs) being assigned as shown in Fig. 1. In Table 1, we summarize the memory allocation for quasi-cyclic LDPC(16935, 13550) code, where we use the following notation: MEM B and MEM C denote the memories used to store bit node and check node edge values; MEM E stores the codeword estimate; MEM I stores the initial LLRs, and MEM F stores final LLRs (required in bit decision step). When RC-min-sum algorithm is used, the MEM B block is not needed at all. Finally, since v-node update rule does not exist in RC-min-sum algorithm, the decoding latency will be lower. Although exact latency improvement is dependent on the implementation platform, our study indicates that proposed RC-min-sum algorithm has lower complexity compared to conventional min-sum algorithm and SPA.

Table 1: Memory allocation requirements of LDPC(16935, 13550) code of column-weight 3 (for $p = 1129$ and $[b] = 15$)

<table>
<thead>
<tr>
<th>Name/ MEM</th>
<th>EM B</th>
<th>EM C</th>
<th>EM E</th>
<th>M 1</th>
<th>M 2</th>
<th>M 3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Data word (bits)</td>
<td>8</td>
<td>11</td>
<td>8</td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Address word (bits)</td>
<td>16</td>
<td>16</td>
<td>16</td>
<td>15</td>
<td>15</td>
<td></td>
</tr>
<tr>
<td>Memory block size (words)</td>
<td>50</td>
<td>50</td>
<td>935</td>
<td>805</td>
<td>805</td>
<td>16</td>
</tr>
</tbody>
</table>

Fig. 1. Assignment of v-nodes and c-nodes to BPEs and CPEs, respectively. $I$ denotes the identity matrix of size $p 	imes p$ ($p$ is a prime), $P$ is the permutation matrix given by $P = \begin{pmatrix} p_{ij} \end{pmatrix}$ for $p_{ij} = 1$ (zero otherwise), and $r$ and $c$ represent the number of block-rows and block-columns in parity-check matrix. The set of integers $S$ are carefully chosen from the set $\{0,1,\ldots,p-1\}$ so that the cycles of short length (4 and 6) are avoided.

Fig. 2. BER performance of RC LDPC decoding algorithms in comparison with SPA, Min-sum-CT: min-sum-plus-correction-term algorithm. (The constant in front of algorithm refers to optimum attenuation factor. The attenuation factor in SPA is introduced in box plus operator only.)

We turn our attention now to the BER performance evaluation of proposed reduced complexity algorithms. In Fig. 2, we show the results of Monte Carlo simulations for different LDPC decoding algorithms and optimum attenuation factors (obtained numerically). The large-girth LDPC(16935, 13550) code is used in simulations. It is interesting to notice that min-sum-plus-correction-term algorithm faces negligible performance loss, which is in
agreement with [2,4]. The min-sum algorithm with optimum attenuation factor $\alpha = 0.8$ shows similar performance as SPA, while RC-min-sum with optimum attenuation factor of 0.44 faces only 0.46 dB degradation at BER of $10^{-9}$. The storage complexity and latency of optimally attenuated RC-min-sum algorithm are much lower, which makes the proposed algorithm as an excellent candidate for high-speed implementation. The optimally attenuated RC-APP algorithm performs 0.2 dB worse than optimally attenuated RC-min-sum algorithm. It is interesting to notice that it is possible to improve performance of SPA by 0.1 dB at BER $= 10^{-9}$ for attenuation factor of 0.9. In Fig. 3 we study the influence of quantization effect on BER performance of various decoders. When 4 bits (3 bits for magnitude and one bit for sign) are used, there is only extra 0.05 dB penalty for both 0.8-min-sum and 0.4-RC-APP algorithms (at BER of $10^{-7}$). When 3 bits are used (2 for magnitude and 1 for sign), the corresponding degradations are 0.26 dB and 0.38 dB respectively. Finally, when only 1 bit is used for magnitude and 1 for sign, 0.8-min-sum algorithm exhibits about 0.89 dB degradation, while degradation for 0.4-RC-APP is much worse. Given this description of proposed RC LDPC decoding algorithms, in next Section we study their application in PolMUX multilevel coded modulation with coherent detection.

![Figure 3. Quantization effect influence on BER performance.](image)

### 3. PolMUX IPQ coded-modulation based on large-girth LDPC codes and RC decoders

The PolMUX IPQ-based coded modulation scheme suitable for beyond 400 Gb/s per wavelength optical transmission is shown in Fig. 4. The $m_x + m_y$ (index $x$ ($y$) corresponds to $x$-($y$-) polarization) independent data streams are encoded using different LDPC codes of code rates $R_i = K_i/N$ ($i \in \{x,y\}$), where $K_i$ ($K_x$) denotes the number of information bits used in the binary LDPC code corresponding to $x$- ($y$-) polarization, and $N$ denotes the codeword length. The $m_x$ ($m_y$) input bit streams from $m_x$ ($m_y$) different information sources, pass through identical encoders that use LDPC codes with code rate $R_x$ ($R_y$) designed using a quasi-cyclic code design [2]. The outputs of the encoders are then bit-interleaved by an $m_x \times N$ ($m_y \times N$) bit-interleaver where the sequences are written row-wise and read column-wise from a block-interleaver. The mapper maps each $m_x$ ($m_y$) bits, taken from interleaver, into a $2^{m_x}$ ($2^{m_y}$) IPQ signal constellation point based on the LUT, which is for $M = 32$ given in Table 2 ($m_i$ denotes the $i$th circle radius, $L_i$ denotes the number of constellation points per $i$th circle, $r_i$ denotes the decision regions in amplitude coordinate). The corresponding constellation diagram is shown in Fig. 5, as we described in [3]. The IPQ mapper $x$ ($y$) assigns $m_x$ ($m_y$) bits to a constellation point represented in polar coordinates as $s_{x,y} = [s_{x,y}]\exp[j\phi_{x,y}] = [s_{x,y}]\exp[j\phi_{x} + j\phi_{y}]$, where $s_{x,y}$ one output of IPQ mapper is used as input of amplitude modulator (AM), while the second output is used as input to phase modulator (PM), as shown in Fig. 4(a). Notice that we use $(m_x + m_y)$ encoders/decoders operating in parallel at data rate of $R_b$ instead of only one encoder/decoder operating at date rate of $(m_x + m_y)R_b$. At the receiver side (see Fig. 4(b)), the outputs at I- and Q-branches in two polarizations, are sampled at the symbol rate, while the
symbol LLRs are calculated by $\lambda(s) = \log[P(s|\tilde{r})/P(s|r)]$, where $s$ and $r$ denote the transmitted signal constellation point and received symbol at time instance $i$ (in either $x$- or $y$-polarization), respectively, and $s_0$ represents the reference symbol. The turbo equalization (TE) principle is used to compensate for various channel impairments such as PMD, residual chromatic dispersion, and fiber nonlinearities [2]. Since the turbo equalization is not the main topic of this paper, we assume that channel impairments are ideally compensated for. The results of simulations of PolMUX based LDPC-coded IPQ scheme with 50 GS/s in symbol rate are shown in Fig. 6. Corresponding encoders, decoders, mappers and demappers operate at data rate of 50 Gb/s. Notice that proposed LDPC decoding schemes are independent on data rate. The aggregate data rate of this particular simulation example is obtained as $2 \times 5 \times 0.8 \times 50 \text{ Gb/s} = 400 \text{ Gb/s}$ (the factor 2 originates from two orthogonal polarizations, the factor 5 from 5 bits carried per single 32-IPQ symbol, and the factor 0.8 from code rate). The NCG at BER of $3 \times 10^{-9}$, when min-sum-with-correction-term algorithm is used, is 11.6 dB. Larger coding gains can be expected at lower BERs. The optimally attenuated min-sum algorithm performs comparable to min-sum-with-correction-term algorithm. The RC-min-sum algorithm provides the NCG of 11 dB. This RC decoding based scheme, therefore, represents an excellent candidate to be used for 400G Ethernet technologies.

![PolMUX PEG-LDPC-coded IPQ modulation scheme](diagram)

Fig. 4. PolMUX PEG-LDPC-coded IPQ modulation scheme: (a) transmitter and (b) receiver configurations. MAP: maximum a posteriori probability.

<table>
<thead>
<tr>
<th>$i$</th>
<th>1</th>
<th>2</th>
<th>3</th>
<th>4</th>
</tr>
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<tbody>
<tr>
<td>$r_i$</td>
<td>0.896</td>
<td>1.733</td>
<td>4.5</td>
<td></td>
</tr>
<tr>
<td>$m_i$</td>
<td>0.547</td>
<td>1.269</td>
<td>2.181</td>
<td></td>
</tr>
<tr>
<td>$L_i$</td>
<td>6</td>
<td>12</td>
<td>14</td>
<td></td>
</tr>
</tbody>
</table>

Table 2: Specifications for 32-IPQ-based modulation

![32-IPQ constellation](diagram)

Fig. 5. 32-IPQ constellation.
4. Conclusions

In this paper, we proposed two RC LDPC decoders, suitable for use in ultra-high-speed serial optical transmission: (i) attenuated RC min-sum algorithm and (ii) RC APP algorithm. We show that optimally attenuated RC min-sum sum algorithm performs only 0.46 dB (at BER = $10^{-9}$) worse than the conventional sum-product algorithm, when used in combination with large-girth LDPC codes. The RC APP algorithm performs 0.2 dB worse than RC min-sum algorithm. The proposed algorithms simplify the implementation complexity and have lower storage memory requirements and lower latency, and can be used to support ultra-high-speed implementation. We further evaluate the proposed algorithm for use in PolMUX multilevel coded modulation with coherent detection, in combination with PolMUX 32-IPQ-based signal constellation. We show that low BERs can be achieved for medium optical SNRs, while achieving the NCG above 11 dB.

Acknowledgments

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Fig. 6. BER performance of PolMUX LDPC-coded IPQ scheme. CT: correction term.