Proposal for Beyond 100-Gb/s Optical Transmission Based on Bit-Interleaved LDPC-Coded Modulation

Ivan B. Djordjevic, Member, IEEE, Milorad Cvijetic, Senior Member, IEEE, Lei Xu, and Ting Wang

Abstract—An iterative bandwidth-efficient coded modulation scheme based on bit-interleaving low-density parity-check (LDPC) codes, and M-ary differential phase-shift keying is proposed. A bit-interleaved LDPC-coded scheme, carrying 3 bits/symbol, provides the coding gain of 8.3 dB at a bit-error rate (BER) of $10^{-12}$. The expected coding gain at BER of $10^{-12}$ is 12.8 dB. Possible applications include 100G Ethernet, and high-speed (> 100 Gb/s) long-haul transmission.

Index Terms—100G Ethernet, bit-interleaved coded modulation, direct detection, high-speed optical transmission, low-density parity-check (LDPC) codes, optical communications.

I. INTRODUCTION

Ethernet was initially introduced as a communication standard for connection of hosts in a local area network [1]. Thanks to the low-cost and simplicity compared to other protocols, it has rapidly evolved and has already been used to enable campus-size distance connections, and beyond, in metropolitan area networks [1]. The 100-Gb/s transmission is envisioned as a technology for the next generation of Ethernet, because traditionally the Ethernet data rates have grown in ten fold increments [1]–[3]. All electrically time-division-multiplexed (ETDM) transceivers operating at 100 Gb/s, although already commercially available, are still expensive so that alternative approaches to enable a 100-Gb/s transmission using commercially available components operating at lower speed are intensively sought [3].

In this letter, we propose an alternative technique to 100-Gb/s ETDM, which achieves 100-Gb/s optical transmission using bit-interleaved low-density parity-check (LDPC)-coded modulation (BI-LDPC-CM), M-ary differential phase-shift keying (DPSK) ($M = 8, 16$), and commercially available modulators and photodetectors operating at 40 Gb/s. The receiver architecture is composed of two ingredients, a demapper and an LDPC decoder. The demapper is implemented as a posteriori probability (APP) demapper, and LDPC decoder is based on an efficient implementation of sum-product algorithm [4]. To improve the bit-error-rate (BER) performance, the iterative demapping and decoding is employed [5]. To study the convergence behavior, the extrinsic information transfer (EXIT) chart analysis is applied [6]. To keep the complexity of the LDPC decoder reasonably low for high-speed implementation, the structured LDPC codes of girth-8 are applied. The proposed BI-LDPC-CM scheme is easier to implement than the recently proposed multilevel coding (MLC) scheme with LDPC component codes [8], because the same LDPC code is used for different source streams, and at the same time offers higher spectral efficiency. In our approach, described in Section II, modulation and coding are performed in a unified fashion so that, effectively, the transmission, signal processing, detection, and decoding are done at lower symbol rates (e.g., 40-Giga symbols/s) where the influence of intrachannel nonlinearities and polarization-mode dispersion (PMD) is less severe.

II. HIGH-SPEED OPTICAL TRANSMISSION BASED ON BI-LDPC-CM AND M-ARY DPSK

The transmitter and receiver architectures of the proposed BI-LDPC-CM scheme are shown in Fig. 1(a) and (b), respectively. The source bit streams coming from $m$ information sources (e.g., carrying 40-Gb/s traffic) are encoded using identical $(n, k)$ LDPC codes of code rate $r = k/n$ ($k$ is the number of information bits, $n$ is the codeword length). The interleaver, implemented as $m \times n$ block-interleaver, collects $m$ codewords written row-wise. The mapper accepts $m$ bits from the interleaver at the time column-wise and determines the corresponding $M$-ary $(M = 2^n)$ signal constellation point, using differential encoding: at each $l$th transmission interval, the data phasor $\phi_l = \phi_{l-1} + \Delta \phi_l$ is sent, where $\Delta \phi_l \in \{0, 2\pi/M, \ldots, 2\pi(M-1)/M\}$. Three different maps are considered in this letter: gray, anti-gray, and natural mapping. The transmitted signal may be written in complex notation as

$$s(t) = \sum_{l} I_l g(t - lT) + j Q_l g(t - lT)$$

(1)

where $I_l$ and $Q_l$ are equal to (assuming $M$-ary DPSK signaling) $\cos(\phi_{l-1} + \Delta \phi_l)$ and $\sin(\phi_{l-1} + \Delta \phi_l)$, respectively. $g(t)$ denotes a transmitted signal pulse shape. Notice that the MLC scheme, proposed in [8], employs different $(n, k_s)$ LDPC

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I. B. Djordjevic is with the Department of Electrical and Computer Engineering, University of Arizona, Tucson, AZ 85721 USA (e-mail: ivan@ece.arizona.edu).

M. Cvijetic is with NEC Corporation of America, Herndon, VA 20171 USA.

L. Xu and T. Wang are with NEC Laboratories America, Princeton, NJ 08540 USA.

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codes (k_i-dimensionality of i-th component LDPC code), and it is able to carry \( \sum k_i/\eta \) bits per symbol. This is generally smaller than \( m \), number of bits/symbol of bit-interleaved scheme proposed in this letter. Moreover, the use of the same LDPC code allows iterating between APP demapper and LDPC decoders, improving the BER performance. The source bits may originate from a single source as well, and in that case only one LDPC encoder/decoder is required. It is also possible to multiplex the bits from `m` source channels into one data stream, and use only one LDPC code, in a fashion similar to that proposed for wireless communications [5]. However, the LDPC encoder/decoder operating speed would be \( mR_b (R_b/\eta \text{ bit rate}) \), which is too high for today’s available high-speed electronics. Such a solution also requires the use of additional interleaver and deinterleaver. Another important fact is that iterating between LDPC decoders and demapper is also possible in MLC schemes. However, the multistage decoding algorithm, in which decisions from lower decoding stages are passed to higher stages, must be employed, which introduces inherently large decoding delay to be of practical importance for very high-speed applications, such as optical communications. Other modulation schemes, such as an \( M \)-ary differential quadrature-amplitude modulation (DQAM), are also applicable. In DQAM, different signal constellation points are to be transmitted with different amplitudes, and as such are more sensitive to self-phase modulation and intrachannel four-wave mixing, for symbol rates at 40-Giga symbols/s and above. Moreover, to exploit fully the advantages of DQAM, a modified block differential encoding, which accounts for the noncoherent metric, is to be considered (see [8], and references [18] and [19] therein). This approach increases the transmitter/receiver complexity and reduces the overall code rate.

At the receiver side, for the receiver input \( E_t = |E_t| \exp (j\theta_t) \), the outputs of upper- and lower-branches are proportional to \( \text{Re}\{E_t E_{t-1}^*\} \) and \( \text{Im}\{E_t E_{t-1}^*\} \), respectively. Let \( r = (r_I, r_Q) \) represent the received signal constellation point, with \( r_I \) and \( r_Q \) being the samples of upper- and lower-branches, respectively, at the \( i \)-th symbol interval; let \( c = (c_0, c_1, \ldots, c_{m-1}) \) represent the binary sequence at the output of interleaver, which is mapped into \( s = (I_s, Q_s) \) signal constellation point. The APP demapper symbol log-likelihood ratios (LLRs) can be determined as

\[
\lambda (s) = \log \frac{P(s = s_0 | r)}{P(s \neq s_0 | r)}
\]

(2)

where \( P(r|s) \) is determined using Bayes’ rule

\[
P(s|r) = \frac{P(r|s) P(s)}{\sum_{s'} P(r|s') P(s')}
\]

(3)

In (3), \( P(r|s) \) is estimated by determination of histograms, by propagating sufficiently long training sequence. \( P(s) \) denotes the \textit{a priori} probability of symbol \( s \), whose LLR \( \lambda_a (s) \) is determined from LDPC decoders extrinsic LLRs, \( L_{D_{De}} (c) \), by

\[
\lambda_a (s) = \log P(s) = \sum_{j=0}^{m-1} (1 - c_j) L_{D_{De}} (c_j).
\]

(4)

(\( s_0 \) is a referent symbol.) The bit LLRs are determined from symbol LLRs by

\[
L (\hat{c}_j) = \log \sum_{s_0=0}^{s_0_{\text{max}}} \exp [\lambda (s_0)] \sum_{s_0_{\text{max}}+1}^{s_0_{\text{max}}} \exp [\lambda (s)]
\]

(5)

The LDPC decoder is implemented, as mentioned in Section I, by employing an efficient implementation of sum-product algorithm [4]. The LDPC decoders extrinsic LLRs \( L_{D_{De}} \) are fed to the APP demapper as \textit{a priori} LLRs \( L_{D_{Ma}} \), by using (4), and substituting (4) into (3). The iteration between the APP demapper and LDPC decoder is performed until the maximum number of iterations is reached or the valid code-words are obtained.

To study the convergence properties of the proposed BI-LDPC-CM scheme, the EXIT chart analysis is employed as explained in [6]. To determine the mutual information (MI) characteristics of the demapper, we model \textit{a priori} input LLR \( L_{D_{Ma}} \) as a conditional Gaussian random variable [6]. The MI between \( c \) and \( L_{D_{Ma}} \) is determined numerically as explained in [6]. Similarly, the MI \( L_{I_{LMa}c} \) between \( c \) and \( L_{LMa} \) is calculated numerically, but with the probability density function of \( c \) and \( L_{LMa} \) determined from histogram obtained by Monte Carlo simulation, as explained in [6]. By observing that \( L_{LMa} \) is a function of the MI \( I_{LMa},a \) and optical signal-to-noise ratio (OSNR) in decibels, the demapper EXIT characteristic (denoted by \( T_M \)) is given by \( I_{LMa} = T_M (I_{LMa},a, \text{OSNR}) \). The EXIT characteristic of LDPC decoder (denoted by \( T_D \)) is defined in a similar fashion as \( T_{D_{De}} = T_D (I_{LD_{De},a}) \), where \( I_{D_{De}} \) is MI between \( c \) and the decoder extrinsic LLRs, while \( I_{LD_{De}} \) is MI between \( c \) and demapper \textit{a priori} LLRs (demapper extrinsic LLRs). The “turbo” demapping-based receiver operates by passing extrinsic LLRs between demapper and LDPC decoder. The iterative process starts with an initial demapping in which \( L_{D_{Ma}} \) is set to zero, and as a consequence \( I_{LMa,a} = 0 \). The demapper output LLRs, described by \( I_{LMa,e} = I_{LD_{Ma},e} \), are fed to LDPC decoder. The LDPC decoder output LLRs, described by \( I_{LD_{De}} = I_{LD_{De},e} \), are fed to the APP demapper. The iterative procedure is repeated until the convergence or until the maximum number of iterations has been reached. This procedure is illustrated in Fig. 2, where the APP demapper and LDPC decoder EXIT charts are combined together. Eight-DSPK, 16-DPSK, and three different mappings are observed: natural, gray, and anti-gray. Different mappings produce the EXIT curves with different slopes. The existence of “tunnel” between the demapping and decoder curves suggests that iteration between demapper and decoder will result in successful decoding. The smallest OSNR at which the iterative scheme converges defines the threshold or pinch-off limit [6], which is in the case of 16-DPSK about 3 dB worse compared to 8-DPSK.
III. SIMULATION RESULTS AND CONCLUSION

The results of simulations for an additive Gaussian noise (AWGN) channel model are shown in Fig. 3 for 30 iterations in the sum-product algorithm. The information symbol rate is set to 40-Giga symbols/s, 8-DPSK (on the left) and 16-DPSK (on the right) are employed in simulations, and maximum aggregate bit rate is 120 and 160 Gb/s, respectively. The improvement (over the first iteration) after the tenth outer iteration for the gray mapping rule is insignificant, which was expected from the EXIT chart shown in Fig. 2. The EXIT chart for the gray demapper is a horizontal line suggesting that iteration between the demapper and the LDPC decoder helps very little in BER performance improvement. On the other hand, the iteration between the demapper and decoder in the case of anti-gray mapping provides more than 1-dB improvement at BER $= 10^{-7}$. However, for 8-DPSK signaling, the anti-gray turbo demapper performs comparable to the gray demapper-decoder after the first iteration. The gray-mapping-based turbo demapper (for 8-DPSK) provides the coding gain of 8.3 dB at BER of $10^{-7}$. The expected coding gain at BER of $10^{-12}$ is about 12.8 dB. With the gray-mapping-based BI-LDPC-CM scheme, a transmission distance larger than 2760 km is possible. The proposed scheme is also suitable for 100-Gb/s Ethernet. By using 16-DPSK and BI-LDPC-CM, it is possible to achieve 160-Gb/s transmission using commercially available electronics operating at 40 Gb/s. Once the ETDM technology at 100 Gb/s becomes mature enough, the scheme proposed in this letter can be used to achieve $\geq$400-Gb/s transmission.

REFERENCES