PMD Compensation by LDPC-Coded Turbo Equalization

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***Abstract*—A turbo equalization scheme suitable for electronic polarization-mode dispersion compensation based on low-density parity-check coding and the Bahl–Cocke–Jelinek–Raviv (BCJR) equalizer is proposed. For reasonable BCJR equalizer complexity, the differential group delay of up to three bit-periods can be compensated.**

***Index Terms*—Fiber-optics communications, low-density parity-check (LDPC) codes, polarization-mode dispersion (PMD), turbo equalization.**

I. Introduction

AT HIGH transmission rates, the signal quality of the wavelength-division-multiplexed optical channels is degraded significantly due to linear and nonlinear effects, in particular fiber nonlinearities and polarization-mode dispersion (PMD) [1]–[4]. In contrast to chromatic dispersion impairments, the PMD is time variant and stochastic in nature, making the PMD compensation more challenging. Several electrical and optical compensators have been proposed recently [1], [2]. Because the electrical PMD compensators rely on fast electronic signal processing that potentially can be implemented as low-cost integrated devices, we are facing a growing research attention in different electronic PMD equalization techniques [1]–[3].

In this letter, a particular turbo equalization scheme, suitable for electronic PMD compensation, based on Bahl–Cocke–Jelinek–Raviv (BCJR) equalizer [4], [5] and a novel class of low-density parity-check (LDPC) codes, is proposed. We show that for reasonable BCJR equalizer complexity, the first-order PMD with differential group delay (DGD) up to three bit periods can be compensated for. Notice that turbo equalization based on *convolutional codes*, introduced in [6], has already been considered for PMD compensation [3]. Unfortunately, the turbo equalization scheme based on convolutional codes [6] exhibits the error floor phenomena at bit-error ratios (BERs) about 10^{-6} (see [3, Fig. 17]). In several recent papers (see [7], and references therein), we have shown that iteratively decodable LDPC codes outperform turbo product codes (TPCs) in terms of BER performance. The decoder complexity of these codes is comparable to (or lower than) that of TPCs, and significantly lower than that of serial/parallel concatenated turbo codes. The main difference between the BCJR and Viterbi equalizers is that in addition to detected sequence, the BCJR equalizer provides the bit soft reliabilities [log-likelihood ratios (LLRs)] required for iterative decoding. Iterative decoding and LDPC coding is currently the most advanced forward-error correction (FEC) approach, but its power can be fully exploited only if the soft bit reliabilities are supplied to the decoder. The extrinsic information transfer chart analysis [8] is used to select the structured LDPC codes suitable for turbo equalization of PMD. To facilitate the implementation, a novel class of structured LDPC codes, designed using the concept of product of orthogonal arrays [9], is introduced.

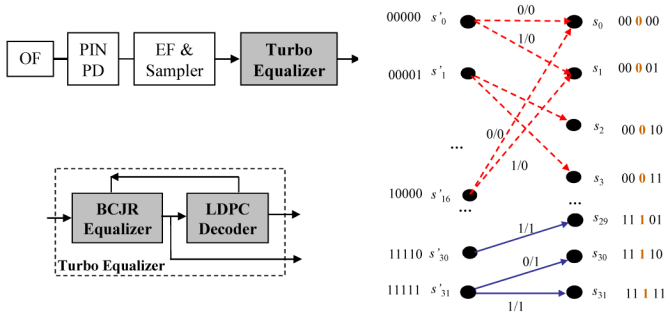

Fig. 1. (left) Receiver and PMD compensator architectures (OF: optical filter; PD: photodetector; EF: electrical filter), and (right) trellis for $2m + 1 = 5$.

II. LDPC-Coded PMD Turbo Equalizer

The return-to-zero ON–OFF keying (RZ-OOK) receiver and turbo equalizer configurations are shown in Fig. 1(left). The turbo equalizer is composed of two components: 1) the BCJR equalizer, and 2) LDPC decoder. The main idea behind this proposal is to use the BCJR equalizer to partially cancel the intersymbol interference due to PMD, to reduce the BER down to $10^{-3}-10^{-4}$, and feed the LLRs obtained from the BCJR equalizer into an iterative decoder of an LDPC code. If a valid codeword is reached, decoding halts. Otherwise, the sum-product LDPC decoder starts decoding by taking the produced BCJR LLRs as inputs. We refer to this step as an *outer iteration*, to differentiate it from iterations within the sum-product algorithm, which are referred to as *inner iterations*. The *extrinsic* LLRs of the LDPC decoder (the difference of LDPC decoder output and input LLRs) are passed back to the BCJR equalizer as inputs. The BCJR equalizer processes the samples and the LDPC decoder extrinsic LLRs, to provide the initial LLRs for the LDPC decoder. Therefore, the *extrinsic soft information* is iterated between BCJR equalizer and LDPC decoder a certain number of times in a fashion similar to *turbo decoding*. Notice that in the proposed turbo equalizer (composed of BCJR equalizer and

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LDPC decoder), *we do not use the interleaver* (commonly used in turbo equalization schemes, e.g., [3], [6]), to reduce the processing delay and facilitate the implementation at high speed.

For the first-order PMD, the optical channel responses $h_H(t)$ and $h_V(t)$ corresponding to the horizontal and vertical principal states of polarizations are given as [3] $h_H(t) = \delta(t + \Delta\tau/2)$ and $h_V(t) = \delta(t - \Delta\tau/2)$, respectively, where $\Delta\tau$ is DGD.

The BCJR equalizer operates on a *trellis* that is *a discrete dynamical model* of the optical channel, introduced in our recent article [4]. For the complete description of the trellis, the transition probability density functions $p(y_j|u_j) = p(y_j|\boldsymbol{s})$, $\boldsymbol{s} \in \boldsymbol{S}$, are determined from *collected histograms* (y_j represents the sample at the input of the BCJR equalizer that corresponds to the transmitted bit u_j, and $\boldsymbol{S}$ is the set of states in the trellis). The state (bit-configuration) $\boldsymbol{s}$ is determined by m previous and m next bits influencing the observed bit $\boldsymbol{u}_j, \boldsymbol{s} = (u_{j-m}, u_{j-m+1}, \ldots, u_j, u_{j+1}, \ldots, u_{j+m}), u_i \in \{0,1\}$. In Fig. 1(right), an example trellis of memory $2m + 1 = 5$ is shown, which has $2^5 = 32$ states $(\boldsymbol{s}_0, \boldsymbol{s}_1, \ldots, \boldsymbol{s}_{31})$ corresponding to different 5-bit patterns. Starting at a given state, there exist two possible transitions to the next state. The incoming bit determines the first bit in the edge label, and the second bit in the edge label is determined by the central bit of a terminal state (see [4] for calculation of LLRs).

We are turning our attention now to the design of LDPC codes suitable for use in turbo equalization of PMD. The LDPC codes employed in this letter are designed based on the *product of I orthogonal arrays*, the concept introduced by Bush in 1952 [9]. An *orthogonal array* [9] of size N, with k constraint, q levels, strength t, and index λ, denoted as $\lambda-\mathrm{OA}(N,k,q,t)$, is defined as a $k \times N$ matrix A with entries from a set of $q(\geqslant 2)$ elements such that any $t \times 1$ column vector in $t \times N$ submatrix of A is contained λ times. It has been shown in [9] that the existence of orthogonal arrays $\mathrm{OA}(N_i, k_i, q_i, t)(i = 1, 2, \ldots, I)$ implies the existence of the orthogonal array $\mathrm{OA}(N, k, q, t)$, where $N = N_1 N_2 \cdots N_I, q = q_1 q_2 \cdots q_I$, and $k = \min(k_1, k_2, \ldots, k_I)$. Notice that entries of an orthogonal array obtained as the product of I one-dimensional orthogonal arrays is I-dimensional. For example, let us observe the orthogonal arrays OA(4,3,2,2) and OA(9,4,3,2)

$$\begin{array}{l}\mathrm{OA}(4,3,2,2):\\ \quad 0\ 1\ 0\ 1\\ \quad 0\ 1\ 1\ 0\\ \quad 0\ 0\ 1\ 1\\ \mathrm{OA}(9,4,3,2):\\ \quad 0\ 1\ 2\ 0\ 1\ 2\ 0\ 1\ 2\\ \quad 0\ 1\ 2\ 1\ 2\ 0\ 2\ 0\ 1\\ \quad 0\ 1\ 2\ 2\ 0\ 1\ 1\ 2\ 0\\ \quad 0\ 0\ 0\ 1\ 1\ 1\ 2\ 2\ 2.\end{array}$$

The product of those two OAs is OA(36,3,6,2) with $k = \min(3,4) = 3$ constraint and $q = 3 \cdot 2 = 6$ levels. Due to the large size of the obtained product array (36), we list only the entries of the first row in OA(36,3,6,2): (0,0) (0,1) (0,2) (0,0) (0,1) (0,2) (0,0) (0,1) (0,2) (1,0) (1,1) (1,2) (1,0) (1,1) (1,2) (1,0) (1,1) (1,2) (0,0) (0,1) (0,2) (0,0) (0,1) (0,2) (0,0) (0,1) (0,2) (1,0) (1,1) (1,2) (1,0) (1,1) (1,2) (1,0) (1,1) (1,2). As expected, the entries in OA(36,3,6,2) are two-dimensional (because $I = 2$), and the levels are denoted by (0,0), (0,1), (0,2), (1,0), (1,1), and (1,2). Let us denote the positions of entries in the first row of OA(36,3,6,2) (given above) by integers $1, 2, \ldots, 36$. The positions of level (0,0) are 1,4,7,19,22, and 25, and correspond to the first row of a parity-check matrix of an equivalent LDPC code. The positions of level (0,1) are 2,5,8,20,23, and 26, and correspond to the second row of a parity-check matrix, etc. Let us now generalize the example above as follows. Assume that entries of $\mathrm{OA}(N_i, k_i, q_i, t)(i = 1, 2, \ldots, I)$ are written as $k_i \times N_i$ matrix $A_i = (a_{\mathrm{mn}}^{(i)})$. The product $\mathrm{OA}(N, k, q, t)$ can be obtained successively by observing the product of two OAs at a time. We will observe the product of the first two OAs [$\mathrm{OA}(N_1, k_1, q_1, t)$ and $\mathrm{OA}(N_2, k_2, q_2, t)$] only to illustrate the idea. If $\mathrm{OA}(N_1, k_1, q_1, t)$ and $\mathrm{OA}(N_2, k_2, q_2, t)$ are represented as matrices $A_1 = (a_{\mathrm{mn}}^{(1)})$ and $A_2 = (a_{\mathrm{mn}}^{(2)})$, then the product $\mathrm{OA}(N = N_1 N_2, k = \min(k_1, k_2), q = q_1 q_2, t)$ can be represented as the $k \times N_1 N_2$ matrix

$$\begin{array}{l}\left(a_{11}^{(1)}, a_{11}^{(2)}\right) \ldots \left(a_{11}^{(1)}, a_{1N_2}^{(2)}\right) \ldots \left(a_{1N_1}^{(1)}, a_{11}^{(2)}\right) \ldots \left(a_{1N_1}^{(1)}, a_{1N_2}^{(2)}\right)\\ \ldots\\ \left(a_{k1}^{(1)}, a_{k1}^{(2)}\right) \ldots \left(a_{k1}^{(1)}, a_{kN_2}^{(2)}\right) \ldots \left(a_{kN_1}^{(1)}, a_{k1}^{(2)}\right) \ldots \left(a_{kN_1}^{(1)}, a_{kN_2}^{(2)}\right).\end{array}$$

Denote the position of entries in every row as $1, 2, \ldots, N_1 N_2$, and $q_1 q_2$-levels as $(0,0), \ldots, (0, q_2 - 1), \ldots, (q_1 - 1, 0), \ldots, (q_1 - 1, q_2 - 1)$. By reading-off positions of levels in every row and writing them as corresponding rows of the parity-check matrix, we are able to create the parity-check matrix of the corresponding LDPC code in a fashion similar to that given in the example above. The code rate of an LDPC code designed using the concept of product of orthogonal arrays is lower bounded by

$$R = \frac{N - \mathrm{rank}\,(H)}{N} \geqslant 1 - \frac{\min(k_1, k_2, \ldots, k_I)\, q_1 q_2 \ldots q_I}{N_1 N_2 \ldots N_I}. \tag{1}$$

Since the product of sizes grows much faster than the product of levels [in (1)], the high code rates LDPC codes can easily be designed. (With $\mathrm{rank}(H)$, we denoted the rank of a parity-check matrix H.) For example, the LDPC code designed using the product of OA(49,8,7,2) and OA(169,14,13,2) has the rate 0.9129, and the codeword length 8281. The girth (the shortest cycle in corresponding bipartite graph [7]) of the proposed LDPC codes is at least six.

In Fig. 2, the BER performance of the proposed LDPC codes (for 30 iterations in sum-product decoding algorithm) are compared against random LDPC codes, RS codes, concatenated RS codes, and TPCs. $R = 0.93$ LDPC code outperforms random $R = 0.936$ LDPC code due to MacKay. The same LDPC code (of rate 0.93) outperforms RS concatenated code of significantly

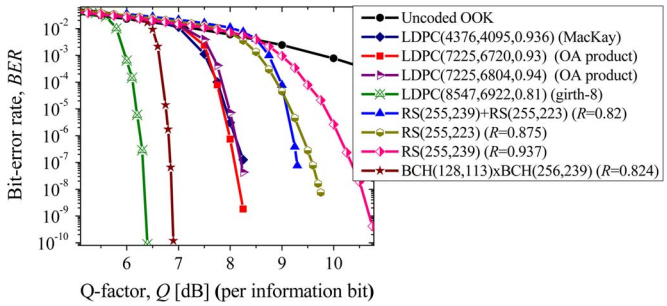

Fig. 2. Proposed LDPC codes against RS, concatenated RS, and TPCs.

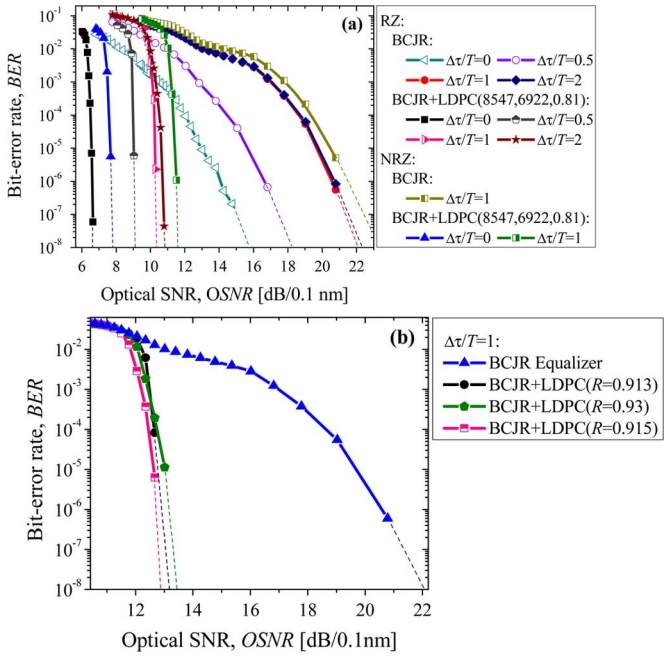

Fig. 3. BER performance of PMD turbo equalizer of trellis memory $2m+1=7$ for different LDPC codes: (a) girth-8 LDPC code, and (b) girth-6 LDPC codes of rates above 0.9.

lower code rate ($R=0.82$) by 1.2 dB at a BER of 10^{-8}. $R=0.81$ LDPC code outperforms $R=0.824$ turbo-product code by more than 0.5 dB at BER of 10^{-8}, and outperforms concatenated RS code ($R=0.82$) by about 3 dB.

III. Numerical Results and Conclusion

The results of simulations, for the amplified spontaneous emission noise dominated scenario, are shown in Fig. 3 for different DGD values and different LDPC codes: (a) girth-8 LDPC code of rate 0.81, and (b) girth-6 LDPC codes of rate above 0.9. RZ-OOK of a duty cycle of 33% is observed, the launched power is set to 0 dBm, and the extinction ratio to 14 dB. The bandwidth of the optical filter is set to $3/T$, and the bandwidth of the electrical filter to $0.65/T$. (For more details on the simulator, an interested reader is referred to [7].) Although the results of simulations are obtained for 40-Gb/s transmission, they are reported in terms of normalized DGD (DGD is normalized with the bit duration), so that the conclusions are applicable for 10-Gb/s transmission as well. Three classes of LDPC codes are considered in simulations. The first class is the girth-8 regular LDPC code (8547,6922) of rate $R=0.81$. The second class is regular girth-6 LDPC codes designed based on the product of two orthogonal arrays: (a) LDPC(8281,7560) of code rate 0.913 [based on product of OA(49,8,7,2) and OA(169,14,13,2)], and (b) LDPC(4096,3813) code of rate 0.93 [based on product of OA(16,5,4,2) and OA(256,17,16,2)]. The third class is girth-6 irregular LDPC(3315,3032) code of rate 0.915 obtained from product of OA(16,5,4,2) and OA(256,17,16,2) by judicially removing the entries in the product OA.

For normalized DGD $\Delta\tau/T=1.0$, the $R=0.81$ LDPC-coded turbo equalizer (for trellis memory $2m+1=7$) provides 11.7-dB improvement over BCJR equalizer at BER of 10^{-8} (10.8 dB in net effective coding gain). The optimum threshold receiver enters the error floor, and any advanced FEC *alone* is not able to operate for that DGD. The LDPC codes of code rate above 0.9 provide about 9-dB improvement over BCJR equalizer at a BER of 10^{-8}. For the nonreturn-to-zero (NRZ) modulation format, also shown in Fig. 3(a) (NRZ pulses were modeled assuming raised-cosine pulse shape with rolloff factor of 0.5), $R=0.81$ LDPC code-based turbo equalizer provides 10.5-dB improvement over BCJR equalizer at a BER of 10^{-8}, which is 1.25 dB worse than that for the RZ modulation format. For normalized DGD $\Delta\tau/T=3.0$, even the BCJR equalizer for trellis memory $2m+1=5$ enters the error floor, while for larger trellis memories it is able to operate properly. For the normalized DGD of 1.0 (and BER of 10^{-8}), the turbo equalizer is 3.7 dB away from the undistorted case, while the normalized DGD of 2.0 has a penalty of 4.2 dB. At a BER below 10^{-12}, much larger coding gains are expected. The simulations are performed for five outer iterations and 25 sum-product algorithm inner iterations. Notice that turbo equalization schemes based on convolutional codes and interleavers exhibit severe error flooring around 10^{-6} (e.g., [3, Fig. 17]), and require additional outer RS code to deal with the error floor phenomena. Simulation results reported in Fig. 2 show that proposed LDPC codes do not the exhibit error floor phenomena down to 10^{-10}. Moreover, we have recently shown in [7] that different classes of LDPC codes developed by our research team do not exhibit the error floor in the region of interest for fiber-optics communications ($<10^{-12}$). Notice also that the proposed LDPC-coded turbo equalizer is able to operate even at normalized DGD $\Delta\tau/T=3.0$ for the trellis memory $2m+1=7$. For trellis memories above $2m+1=7$, soft-output Viterbi equalizer would be a more reasonable choice than the BCJR equalizer. Another important fact is that the proposed LDPC turbo equalizer scheme does not require the use of interleavers, while the other turbo equalization schemes do (see, for example, [3] and [6]).

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