Evaluation of large girth LDPC codes for PMD compensation by turbo equalization

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Abstract: Large-girth quasi-cyclic LDPC codes have been experimentally evaluated for use in PMD compensation by turbo equalization for a 10 Gb/s NRZ optical transmission system, and observing one sample per bit. Net effective coding gain improvement for girth-10, rate 0.906 code of length 11936 over maximum a posteriori probability (MAP) detector for differential group delay of 125 ps is 6.25 dB at BER of 10^{-6}. Girth-10 LDPC code of rate 0.8 outperforms the girth-10 code of rate 0.906 by 2.75 dB, and provides the net effective coding gain improvement of 9 dB at the same BER. It is experimentally determined that girth-10 LDPC codes of length around 15000 approach channel capacity limit within 1.25 dB.

References and links

1. T. Mizuochi, Y. Miyata, T. Kobayashi, K. Ouchi, K. Kuno, K. Kubo, K. Shimizu, H. Tagami, H. Yoshida, H. Fujita, M. Akita, and K. Motoshima, "Forward error correction based on block turbo code with 3-bit soft decision for 10-Gb/s optical communication systems," IEEE J. Sel. Top. Quantum Electron. **10**, 376–386 (2004).
2. I. B. Djordjevic, H. G. Batshon, M. Cvijetic, L. Xu, and T. Wang, "PMD compensation by LDPC coding based turbo equalization," IEEE Photon. Technol. Lett. **19**, 1163–1165 (2007).
3. B. Vasic, I. B. Djordjevic, and R. Kostuk, "Low-density parity check codes and iterative decoding for long-haul optical communication systems," J. Lightwave Technol. **21**, 438-446 (2003).
4. I. B. Djordjevic S. Sankaranarayanan, S. Chilappagari, and B. Vasic, "Low-density parity-check codes for 40-Gb/s optical transmission systems," IEEE J. Sel. Top. Quantum Electron. **12**, 555-562 (2006).
5. M. P. C. Fossorier, "Quasi-cyclic low-density parity-check codes from circulant permutation matrices," IEEE Trans. Inf. Theory **50**, 1788-1793 (2004).
6. O. Milenkovic, I. B. Djordjevic, and B. Vasic, "Block-circulant low-density parity-check codes for optical communication systems," IEEE J. Sel. Top. Quantum Electron. **10**, 294-299 (2004).
7. I. B. Djordjevic, L. Xu, T. Wang, and M. Cvijetic, "Large girth low-density parity-check codes for long-haul high-speed optical communications," in Proc. OFC/NFOEC 2008, San Diego, CA, Feb. 24-28 2008, Paper no. JWA53.
8. R. Tanner, "A recursive approach to low complexity codes," IEEE Trans. Inf. Theory **IT-27**, 533-547 (1981).
9. L. L. Minkov, I. B. Djordjevic, H. G. Batshon, L. Xu, T. Wang, M. Cvijetic, and F. Kueppers, "Demonstration of PMD compensation by LDPC-coded turbo equalization and channel capacity loss characterization due to PMD and quantization," IEEE Photon. Technol. Lett. **19**, 1852-1854 (2007).
10. H. Xiao-Yu et al., "Efficient implementations of the sum-product algorithm for decoding of LDPC codes," in Proc. IEEE Globecom **2**, 1036-1036E (2001).
11. Y. Miyata, W. Matsumoto, H. Yoshida, and T. Mizuochi, "Efficient FEC for optical communications using concatenated codes to combat error-floor," in Proc. OFC/NFOEC 2008, San Diego, CA, Feb. 24-28 2008, Paper no. OTuE4.
12. M. Arabaci, I. B. Djordjevic, and R. Saunders, "FPGA implementation of LDPC decoders for large girth LDPC codes," in preparation.

1. Introduction

Forward error correction (FEC) for optical communication systems is an active research topic in recent years. Both linear and nonlinear effects of signal propagation in fiber can be successfully mitigated using coding techniques, and the importance of coding theory applications in optical communication systems has increased. Iteratively decodable codes have emerged as the most probable successor for the currently employed concatenated Bose-Chaudhuri-Hocquenghem/Reed-Solomon (BCH/RS) codes. Among them, turbo product codes with BCH component codes [1] and LDPC codes [2]-[7] are considered as viable candidates for future optical networks. It has been previously shown that structured LDPC codes are able to match and outperform turbo-product codes in terms of coding gain and decoder complexity [3].

Random LDPC codes provide excellent coding gains, but decoding complexity is too high for practical implementation due to the random structure of their parity-check matrices. To overcome that shortcoming, the structured LDPC codes have been proposed [2]-[7]. On the expense of certain performance deterioration compared to the random LDPC codes, the decoding complexity is low enough to be implemented in hardware. To compensate for the performance loss due to the regularity of the parity-check matrix, different code parameters can be optimized, including the column-weight of the parity-check matrix, the code-word length, the girth (the shortest cycle length) in the corresponding Tanner (bipartite) graph representation of the parity-check matrix, and trapping sets.

The most reliable way of increasing the coding gain of the LDPC codes, without significantly increasing the decoding complexity, is to increase the code girth. In this paper, we have experimentally tested the performance of large girth (g=10) quasi-cyclic (also known as array or block-circulant) LDPC codes. The length of the code is a limiting factor to the large girth as it has been shown in [5]. Moreover, if the quasi-circular structure of the parity-check matrix is to be preserved, the girth cannot be larger than 12 [5]. To design the large girth quasi-cyclic codes, we developed an efficient computer search algorithm. We perform the evaluation of those codes for use in polarization mode dispersion (PMD) compensation. The optical communication systems in the presence of PMD require the use of equalization. By employing the turbo equalization, the equalizer and soft decoder are implemented jointly, leading to the best performance. Capacity limit is approached to approximately 1.25 dB for most of the used codes.

2. Large girth quasi-cyclic LDPC codes

As previously mentioned, the LDPC codes under study in this paper belong to the class of quasi-cyclic (QC) LDPC codes. The parity-check matrix of the LDPC codes considered here can be written in the following form

$$H = \begin{bmatrix} I & I & I & ... & I \\ I & D^{S[1]} & D^{S[2]} & ... & D^{S[c-1]} \\ I & D^{2S[1]} & D^{2S[2]} & ... & D^{2S[c-1]} \\ ... & ... & ... & ... & ... \\ I & D^{(r-1)S[1]} & D^{(r-1)S[2]} & ... & D^{(r-1)S[c-1]} \end{bmatrix} \tag{1}$$

where I is pxp (p is a prime number) identity matrix, D is pxp permutation matrix ($d_{i,i+1}=d_{p,1}$=1, i=1,2,…,p-1; other elements of D are zeros), while r and c represent the number of rows and columns in (1), respectively. The set of integers S are to be carefully chosen from the set {0,1,…,p-1} so that the cycles of short length, in the corresponding Tanner graph representation of (1), are avoided. We have shown in **Error! Reference source not found.** that large girth, g=10, LDPC codes provide excellent improvement in coding gain over

corresponding turbo-product codes (TPCs). At the same time the complexity of LDPC codes is lower than that of TPCs, selecting them as excellent candidates for application to systems for beyond 40 Gb/s transmission. Namely, the minimum distance for an LDPC code is given by the Tanner bound [8]:

$$d \geq \begin{cases} 1 + \dfrac{w}{w-2}\left((w-1)^{\lfloor(g-2)/4\rfloor} - 1\right), & g/2 = 2m+1 \\ 1 + \dfrac{w}{w-2}\left((w-1)^{\lfloor(g-2)/4\rfloor} - 1\right) + (w-1)^{\lfloor(g-2)/4\rfloor}, & g/2 = 2m \end{cases} \tag{2}$$

where g and w are respectively the girth of the LDPC code and the column weight of the parity check matrix. The operator $\lfloor\ \rfloor$ indicates the largest integer that is smaller or equal to the enclosed number. Equation (2) shows that the linear increase in the girth results in exponential increase of the minimum distance. Notice that this bound is tight only for short codes (in the order of hundreds), nevertheless it provides a guideline of how to design the LDPC codes of large minimum distance. For example, by selecting $p=1123$ and $S=\{2, 5, 13, 20, 37, 58, 91, 135, 160, 220, 292, 354, 712, 830\}$ an LDPC code of rate 0.8, girth $g=10$, column weight 3 and length $N=16845$ is obtained.

3. Experimental setup and PMD compensator

The experimental setup used in this paper is shown in Fig. 1. A personal computer via GPIB interface controls the pattern generator (Anritsu MP1763C) for pattern upload and the oscilloscope (Agilent 11982A) for data collection. A zero-chirp Mach-Zehnder modulator (JDSU OC-192) is used for optical modulation of 10Gb/s NRZ electrical signal. Controlled amount of first-order PMD and amplified-spontaneous emission (ASE) noise are introduced with the aid of a PMD emulator (JDSU PE3), and an ASE source. Amplification is done with an erbium doped amplifier (Optigain, Inc. 2000 series), and photo-detection is performed with a detector Agilent 11982A. Constant level of 0dBm is maintained at the laser source output and the optical signal to noise ratio (OSNR) is controlled by a variable optical attenuator (VOA) and monitored with an optical spectrum analyzer. Constant level of -6dBm is maintained at the detector with the second VOA. The oscilloscope is triggered by the pattern generator. The personal computer serves as an LDPC decoder (the hardware is currently in development stage).
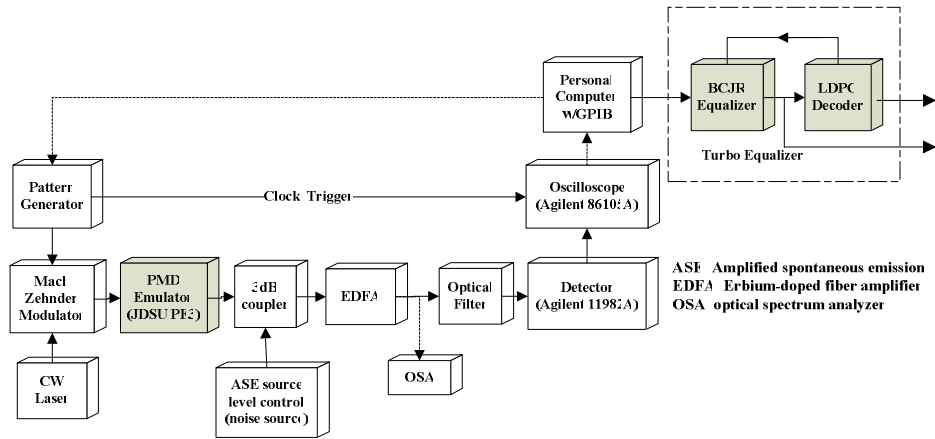

Fig. 1. Experimental setup

The channel was described in terms of a discrete dynamical trellis as we explained in [9]. It was assumed that the trellis memory is $2m+1$, meaning that that every bit x_i from the

transmitted sequence X was affected by the preceding neighboring m ($x_{i-m}, x_{i-m+1}, ..., x_{i-1}$) bits as well as the following neighboring m ($x_{i+1}, ..., x_{i+m}$) bits in the sequence. This subsequence (also known as bit-configuration) defines the state of the trellis as $s=(x_{i-m}, .., x_i, x_{i+1}, ..., x_{i+m})$. The Bahl-Cocke-Jelinek-Raviv (BCJR) algorithm based equalizer provides soft reliabilities for the channel output Y as it operates on the channel trellis. The channel is uniquely defined in any discrete moment in time in terms of the triple {previous state, channel output, next state}.

A requirement for the implementation of MAP detector (equalizer) by means of BCJR algorithm is the knowledge of the channel transition probabilities. The probability density functions (PDFs) for every state were estimated from measurements. The training sequence should be long enough (millions of bits) to provide reliable histograms for PDF estimation. The PDF for a state s that corresponds to the transmitted bit x_i is defined as the conditional probability $p(y_i/s)$, where y_i is the received sample corresponding to x_i. Figure 2 illustrates the trellis concept. Figure 2(a) shows the trellis states for memory $2m+1=5$ and Fig. 2(b) shows the DGD effect on the conditional PDF distribution for two states: $s=$'11011' and '00100'. With increase of the DGD the PDF mean for the first state shifts to the right and the curve becomes wider. This leads to degradation in BER performance, as shown later. Notice that the trellis description shown in Fig. 2(a) is description of the channel used by turbo equalizer. If the memory of the trellis is the same as the channel memory, turbo equalizer should be able completely to eliminate the channel distortions.
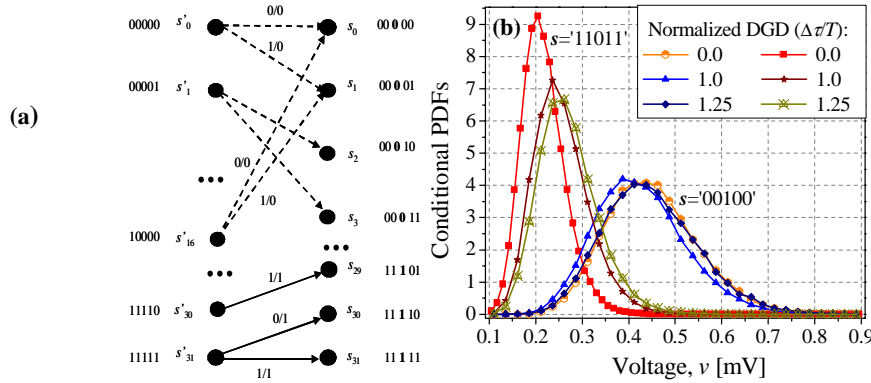

Fig. 2. (a) trellis description ($2m+1=5$), (b) measured conditional PDFs for different DGD values.

4. Experimental results

The performance of several large-girth quasi-cyclic LDPC codes was experimentally evaluated. The LDPC codes under study are listed in Table 1.

Table 1. Tested LDPC codes

LDPC code	Code length	Code rate, R	The girth, g	Column-weight, w
LDPC1	8020	0.950	6	4
LDPC2	11936	0.906	10	3
LDPC3	15328	0.906	10	3
LDPC4	16935	0.800	10	3
LDPC5	4376	0.936	6	4

For comparison purposes the random LDPC5 code (MacKay's random code) is evaluated as well. To guarantee reliable calculation sequence of length approximately 64000 bits is used and acquired multiple times resulting in minimum 10 million test bits per measurement. For every calculation 5 outer and 25 inner iterations were used.

To see how closely the quasi-cyclic LDPC codes are able to approach the channel capacity, in Fig. 3 we show the experimentally determined channel capacity for different values of DGD and different channel memory assumptions. Based on the calculation method we described in [9], we report the independent identically distributed (i.i.d.) channel capacity limits, a lower bound on channel capacity. (This represents the case commonly encountered in practice, since no one is going to transmit the Gaussian-like sequence in practical applications.) The presence of DGD decreases the i.i.d. channel capacity. The memory assumption effect is clearly distinguishable in Fig. 3 - for higher values of DGD, larger memory assumption results in higher i.i.d. channel capacity.
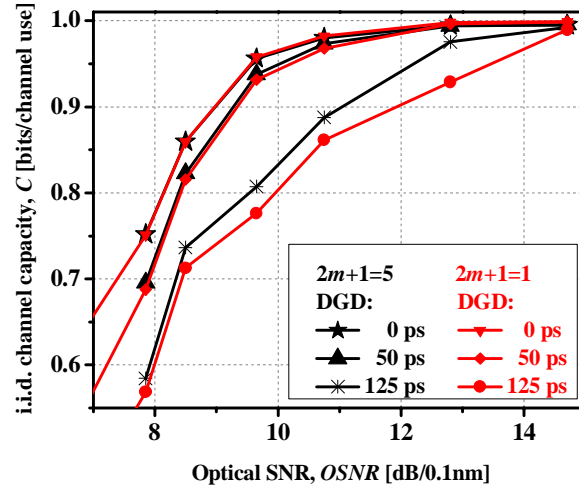

Fig. 3. Channel capacity in the presence of PMD (for an NRZ transmission system operating at 10-Gb/s).
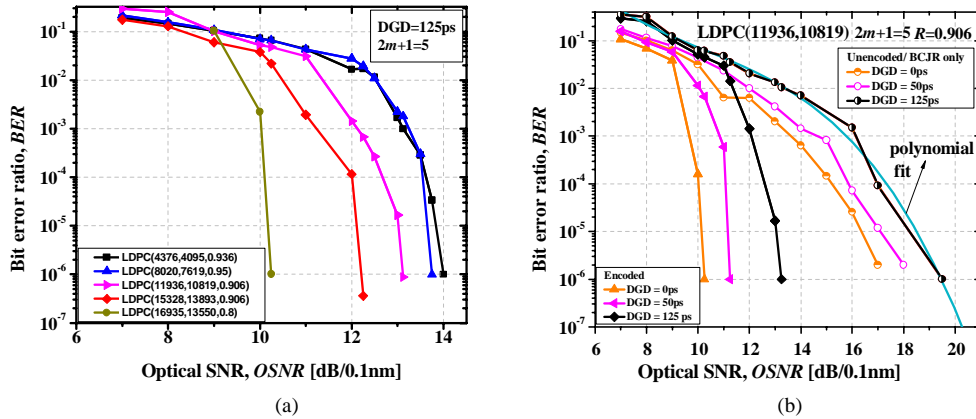

Fig. 4. (a) Performance evaluation of LDPC codes in the presence of constant amount of DGD (125ps). (b) Performance evaluation of LDPC(11936,10819) code of rate $R = 0.906$, for different values of DGD.

Figure 4(a) shows the comparison of the BER performance of the aforementioned codes in the presence of DGD of 125 ps for different OSNR values. Quasi-cyclic LDPC code of girth 6 performs comparable to random MacKay code down to BER of 10^{-4} and outperforms it at lower BER values. QC LDPC2 code of R=0.906 outperforms the random code by 0.75 dB at BER of 10^{-6}. QC LDPC3 code of R=0.906 outperforms LDPC2 code by 1 dB at BER=10^{-6}. QC LDPC4 code of R=0.8 outperforms QC LDPC3 code of R=0.906 by 2 dB at BER=10^{-6}.

The turbo equalizer performance can be evaluated in terms of the channel capacity. The OSNR value for which the i.i.d. channel capacity is the same as the code rate is used as a reference value. The difference between this reference value and the OSNR value at which BER tends to zero presents how far the turbo equalizer from the channel capacity is. QC LDPC2 code is 1.25 dB away from the i.i.d. capacity limit. QC LDPC4 code is 1.27 dB away from the i.i.d. capacity limit. QC LDPC3 code is 1.18 dB away from the i.i.d. capacity limit.

Figure 4(b) shows the comparison of the BER performance of LDPC2 code of rate R=0.906 for DGD of 0ps, 50ps and125ps. The OSNR penalty for DGD of 125ps is 3dB at BER=10^{-6}. Coding gain improvement over BCJR equalizer (with memory $2m+1$=5) for DGD=125ps is 6.25dB at BER=10^{-6}. Larger coding gains are expected at lower BERs. Polynomial fit of 4th order was used to obtain the smoothened version of the measurement curve.

5.   Conclusions

In conclusion, high rate, girth-10, quasi-cyclic LDPC codes were designed, experimentally compared to a random MacKay LDPC code, and evaluated for use in PMD compensation by turbo equalizaiton. Properly designed quasi-cylic code of large girth and sufficient length can match and outperform the random codes. Low decoding complexity implementation is possible due to the low column weigth of these codes (3 or 4) and because of low complexity of min-sum-with-correction-term algorithm [10]. Morever, given the quasi-cyclic structure of the parity-check matrices, the encoder can be implemented using the modulo-2 adders and shift registers. High speed implementation of iterative decoder for this class of LDPC codes can be performed by using either FPGA or VLSI. Our recent paper [12] describes the first step needed for FPGA implementation of turbo equalizer, namely the FPGA implementation of decoders for large girth LDPC codes.

A significant improvement over the results in [9] has been made with the LDPC code of length 16935, rate R=0.8 and girth 10. It provides the net effective coding gain improvement over, BCJR equalizer of 9dB at BER=10^{-6} in the presence of 125ps of DGD. All tested codes were within 1.25dB away from capacity limit. Notice that girth-10 LDPC codes do not exhibit error floor phenomena down to 10^{-15} [11]. That allows extrapolation of results down to BER of 10^{-15}. Such an extrapolation indicates that the net effective coding gain improvement over BCJR equalizer for LDPC4 code is about 12.5 dB at BER of 10^{-15}. Previous simulation results [2] indicate that no significant improvement in perfromance of LDPC-coded turbo equalizer is noticed for the number of inner iterations above 25, and the number of outer iterations above 5. The latency of detection/decoding in turbo equalizer can be reduced by reducing the number of outer iterations, without entering the error floor, at the expense of BER performance degradation.