

# Equivalency-processing parallel photonic integrated circuit (EP<sup>3</sup>IC): equivalence search module based on multiwavelength guided-wave technology

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We present an optoelectronic module called the equivalency-processing parallel photonic integrated circuit (EP<sup>3</sup>IC) that is created specifically to implement high-speed parallel equivalence searches (i.e., database word searches). The module combines a parallel-computation model with multiwavelength photonic integrated-circuit technology to achieve high-speed data processing. On the basis of simulation and initial analytical computation, a single-step multicomparand word-parallel bit-parallel equality search can attain an aggregate processing speed of 82 Tbit/s. We outline the theoretical design of the monolithic module and the integrated components and compare this with a functionally identical bulk-optics implementation. This integrated-circuit solution provides relatively low-power operation, fast switching speed, a compact system footprint, vibration tolerance, and ease of manufacturing. © 2000 Optical Society of America

*OCIS codes:* 250.5300, 230.7390, 200.4560, 200.4540, 200.3050, 200.4740.

## 1. Introduction

Among the integrated optoelectronic systems currently being investigated, two concepts have emerged as forerunners in the optoelectronic processor race. The first of these concepts is based on what are known as smart pixels.<sup>1,2</sup> By use of rudimentary electronic logic for processing and optical sources and detectors for communication, arrays of smart pixels have the capacity for the parallel manipulation of large data sets. The second concept to emerge is called the photonic processor. Here light participates directly in the processor's computation by its being manipulated by various active and passive optical devices. Unlike the smart-pixel approach, a photonic processor processes data at the speed of light, without the need for intermediate conversion to electronics. For example, the Fourier transform operation is naturally suited for

optics and can be implemented with a small number of lenses. Real-time image processing and correlation are two applications that are well documented in the literature.<sup>3</sup>

Photonic processors have also made encouraging progress in optical associative processors for database processing.<sup>4,5</sup> Various designs have been proposed and demonstrated successfully with free-space optics including the optical content-addressable memory<sup>6</sup> and the optical content-addressable parallel processor (OCAPP)<sup>7,8</sup> research systems and Opticomp's Digital Optical Computer II commercial prototype architectures.<sup>9</sup> The most significant demonstrations have involved the implementation of the database-pattern search (equality operation) in which a search word is compared optically with several database words in parallel. However, the microsecond switching speeds of active optical elements such as spatial light modulators (SLM's) cannot realistically compete with the subnanosecond switching speeds of high-performance electronic transistors.

In an effort to increase the number of words that can be compared simultaneously with a database, we have adapted a concept that has become popular in the telecommunications industry, namely, wavelength-division multiplexing. The wavelength-division multiplexing technique increases the communications

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Received May 21 1999; revised manuscript received 6 August 1999.

0003-6935/00/050818-09\$15.00/0

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bandwidth of a channel because it allows for the simultaneous transmission of multiple signals within the same space, each encoded on a separate optical wavelength. Our system, called the multiwavelength OCAPP (MW-OCAPP),<sup>10–13</sup> adapts this concept to optical computing systems by the simultaneous processing of multiple database arguments by the encoding of each on a separate wavelength. The MW-OCAPP offers constant-time multicomparand processing equality searching and efficient use of hardware. Additionally, the MW-OCAPP can be expanded to include the computation of higher-order database operations such as magnitude comparison,<sup>14</sup> union, intersection, and others. We have physically demonstrated the multiwavelength equality operation.<sup>10</sup>

In an attempt to shrink the processor dimensions and enhance dramatically system performance, we developed an integrated-optics version of the MW-OCAPP. We call this new system the equivalency-processing parallel photonic integrated circuit (EP<sup>3</sup>IC). Instead of using bulky discrete laser arrays or SLM's, the EP<sup>3</sup>IC integrates laser sources, modulators, detectors, passive elements, and waveguides on a single monolithic substrate. When compared with discrete optical solutions such as the optical content-addressable memory or the MW-OCAPP, the EP<sup>3</sup>IC allows for the realization of a compact and reliable system that has low power consumption, is vibration insensitive, has a small system size, and is manufacturable. Monolithic integration, in addition, allows the bit-comparison rates of the EP<sup>3</sup>IC to far exceed those that are possible with the MW-OCAPP.

## 2. Equivalency-Processing Parallel Photonic Integrated Circuit

### A. Data Encoding

The EP<sup>3</sup>IC, like the MW-OCAPP, uses several methods for encoding a data plane on a light plane. Binary patterns are represented by spatially distributed, orthogonally polarized logic states. Logical 1 is defined as vertically polarized light and logical 0 as horizontally polarized light. The presence or the absence of light (intensity threshold) within a waveguide indicates the selection or the deselection of words or attributes in the system. The comparand array (CA) is the data array that contains the words to be matched, and the relational array (RA) is the main database that contains the words to match against. Individual tuples in the CA are differentiated from one another by polarization encoding of each on a unique wavelength.

### B. Architecture Overview

The MW-OCAPP is designed to provide efficient parallel data retrieval and processing by means of moving the bulk of the database operations from electronics to optics. The MW-OCAPP uses a multiwavelength encoding scheme to perform multicomparand word-parallel and bit-parallel database operations with an execution time that is indepen-

dent of the data size or the word size. The most fundamental and efficient operation that the MW-OCAPP can perform is the equality operation. This is the operation that the EP<sup>3</sup>IC is designed to implement by use of a guided-wave approach.

The proposed EP<sup>3</sup>IC device is a planar structure composed of an integrated series of optical components connected by waveguides. The operating wavelength range for the EP<sup>3</sup>IC corresponds to the low-loss region of optical silica-based fiber, or 1.4–1.65  $\mu\text{m}$ . One of the most popular systems for emitter–detectors operating at these low-loss wavelengths is the InGaAsP–InP system,<sup>15</sup> which has a bandgap of  $\sim 1.35$  eV. With InP as the base material, several quaternary compounds can be created with customized energy gaps corresponding to the 1.0–1.6- $\mu\text{m}$  range. In addition to the good fundamental optical properties of InP several optoelectronic structures have previously been integrated into this system, demonstrating its practical value. Lasers, modulators, waveguides, and detectors have all been integrated successfully on the same InP substrate.<sup>16–20</sup> There are six integrated subcomponents in the EP<sup>3</sup>IC system: the distributed-feedback laser, the rib waveguide structure, the active polarization-mode converter, the waveguide polarization filter, the waveguide grating demultiplexer, and the photodetectors.

For best presenting the architecture of the EP<sup>3</sup>IC a side-by-side comparison is now made with the bulk-optics implementation in the MW-OCAPP. In the example to follow, two 2-bit words (10, 01) in the CA are compared simultaneously with two 2-bit words (01, 11) in the RA. Where appropriate, simulation and modeling results were included from a beam-propagation simulator called Prometheus<sup>21</sup> and a ray-trace package called ASAP (Advanced Systems Analysis Program).<sup>22</sup>

The first part of the equivalency system as found in the MW-OCAPP is shown in Fig. 1(a). Its purpose is to encode a pixilated two-dimensional optical wave front with the CA to be processed. The rows in the wave front, each encoded on a unique wavelength, represent words to be matched. Polarization encoding of the desired data pattern is employed to differentiate the binary states of each of the pixilated bits.

Using free-space optics, we begin with a multiwavelength source array (SA1) in which each row (which corresponds to a separate tuple) radiates at a different wavelength. This wave front passes through a horizontally oriented polarizer (P1) to reset all the bit positions to the 0 logical state (LP1). Light plane LP1 impinges on an electronically addressable SLM (EASLM), SLM1, that polarization encodes the light passing through it with the CA bit pattern. The resultant light plane, LP2, is called the selection register and represents the optically encoded version of the CA.

Figure 1(b) illustrates the EP<sup>3</sup>IC's monolithic implementation of the architecture shown in Fig. 1(a). The substrate material used in this design is InP. The source array in this case is a distributed-

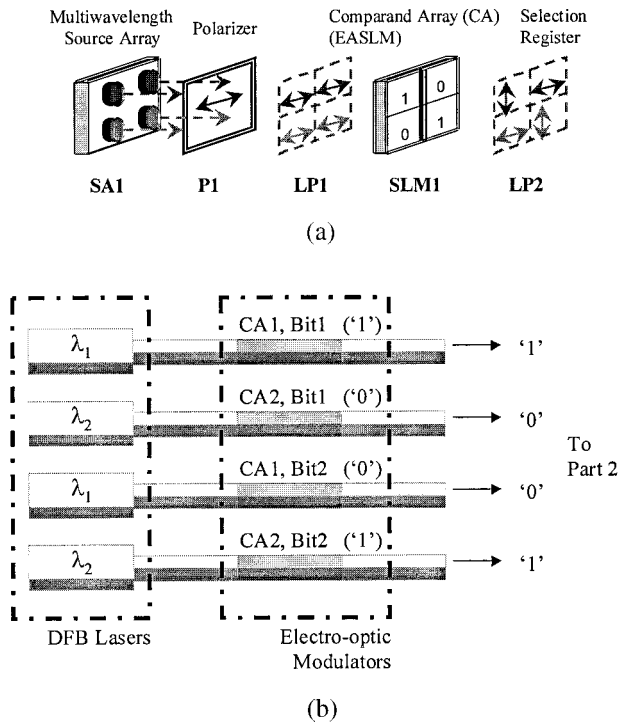


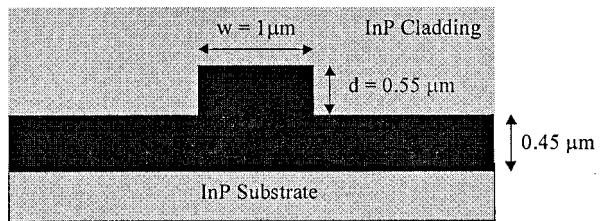
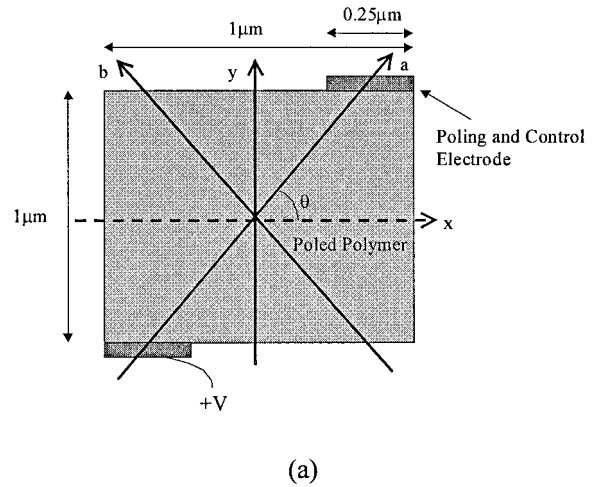
Fig. 1. (a) Part 1 of the MW-OCAPP's equivalency system schematic. (b) EP<sup>3</sup>IC's waveguide equivalent. DFB, distributed-feedback laser; P, polarizer; LP, light plane.

feedback laser array (cw operation) that radiates parallel to the substrate surface.<sup>23</sup> For this example alternating lasers radiate on different wavelengths. Because distributed-feedback lasers emit light that is polarized in the TE orientation (parallel to the substrate surface), all the light is by default in the logical 0 orientation. The lasers are coupled into a single-mode rib waveguide composed of InGaAsP that is designed to be near isotropic.<sup>24</sup>

The next devices in the path are a series of electro-optic modulators<sup>25,26</sup> that encode each of the CA words. Figure 2(a) illustrates the off-axis electrode placement that allows for the poling and the modulation fields to be oriented at approximately 45° with respect to the substrate. These 2-mm-long devices are synchronized by a high-speed electronic host system and operate at the system frequency of 10 GHz. The electro-optic material used is a poled polymer such as poly[N-(4-nitrophenyl)allylamine] or FLAMEL.<sup>27</sup> The lasers are coupled into single-mode rib waveguides composed of InGaAsP with an InP cladding, as shown in Fig. 2(b).

Figure 3 illustrates the second part of the equivalency operation for the MW-OCAPP and the EP<sup>3</sup>IC. Its purpose is to bitwise exclusive-OR (XOR) each tuple in the CA with each tuple in the RA. This produces a logical 1 at every bit position where there is a CA and a RA mismatch.

The encoded light plane LP2 shown in Fig. 1(a) passes through a holographic optical element that duplicates each of the rows with different wavelengths over the full surface of an EASLM (SLM2).



(a)

(b)

Fig. 2. (a) Electrode placement on the electro-optic modulator cross section. (b) The rib waveguide cross section. Waveguide core material, InGaAsP.

Light plane LP3 encoded with the RA to be searched passes through SLM2. The EASLM rotates the polarization(s) of the incident light according to the logic states of its pixels, effectively generating the result of the logical XOR operation in LP4. Light plane LP4 is called the match-compare register (MCR) and contains all the bit-match and bit-mismatch locations of each of the CA and the RA tuple combinations (designated by horizontally and vertically polarized light, respectively).

Figure 3(b) illustrates the EP<sup>3</sup>IC's waveguide equivalent of the second part of the equivalency operation. The corresponding bit positions in each of the words are mixed together with a Y coupler and are then split with a 3-dB Y splitter. These mixed logic states pass through electro-optic modulators that are encoded with the RA pattern. The resulting light plane is the MCR, and this passes on to part 3.

The third and final part of the equivalency unit identifies which combinations of CA and RA tuples are matches. It does so by means of operating on the MCR and converting it to a pixilated map called the equality register (ER), which represents the equivalency results for all the CA and the RA tuple combinations.

Figure 4(a) illustrates the final section of the equality operation. The MCR (LP4) enters and passes through a vertically oriented polarizer (P2) to form

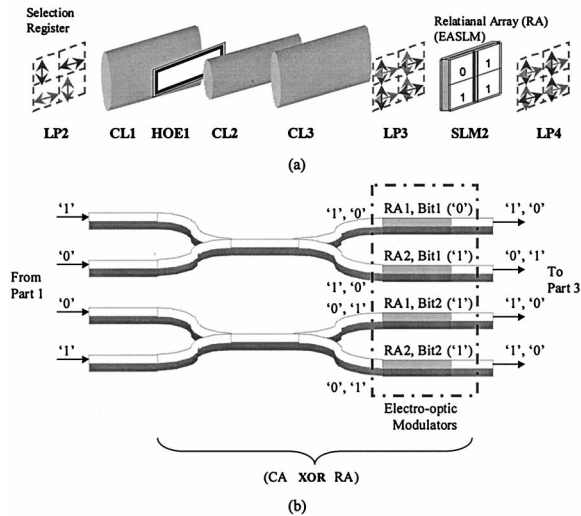


Fig. 3. (a) Part 2 of the MW-OCAPP's equivalency system schematic. (b) EP<sup>3</sup>IC's waveguide equivalent. The first state in the logic pairs following the Y splitter corresponds to  $\lambda_1$ , and the second state in the pairs corresponds to  $\lambda_2$ .

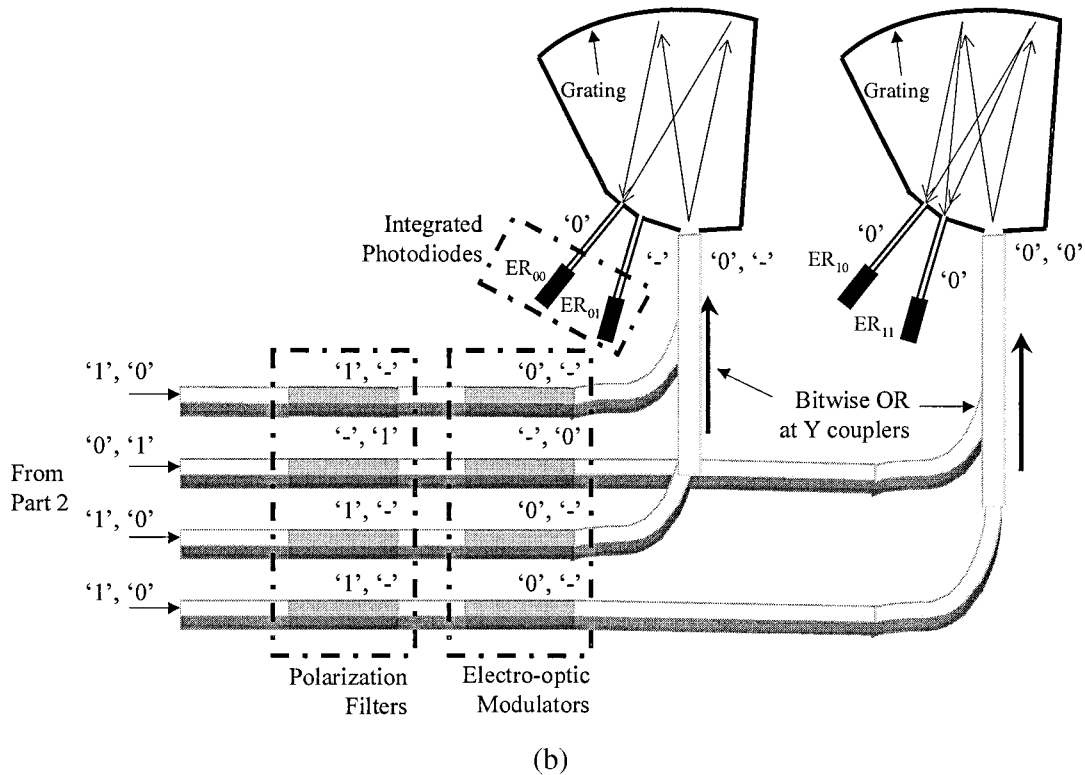
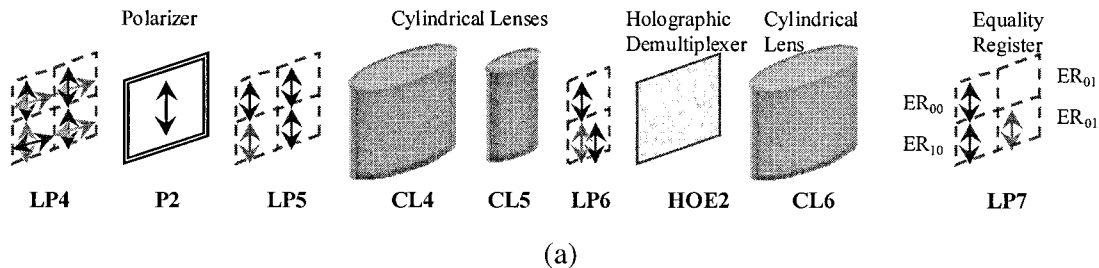


Fig. 4. (a) Part 3 of the MW-OCAPP's equivalency system schematic. (b) The EP<sup>3</sup>IC's waveguide equivalent. The dashes following the polarization filter indicate the absence of light for a particular wavelength in a guide.

LP5. LP5 contains an illuminated pixel corresponding to all bit-mismatch positions. LP5 is funneled down to a single column by cylindrical lenses CL4 and CL5. This single column (LP6) must now be wavelength demultiplexed into a plane that has a pixel-count width equal to the number of tuples in the CA. This can be accomplished with a holographic optical element (HOE2) that is fabricated to deflect light at an angle that is a function of its wavelength. Cylindrical lens CL6 collimates the light exiting HOE2 and produces the ER (LP7). Figure 5 illustrates a photograph of the demonstration system that implements the MW-OCAPP's equality operation.<sup>10</sup>

Figure 4(b) illustrates the EP<sup>3</sup>IC's equivalent waveguide approach for the final part of the equality operation. The MCR from part 2 enters and passes through integrated TM-pass polarization filters. The technology chosen here is a broadband filter that uses a thin discontinuous silver film that is placed between the waveguide core and the cladding.<sup>28</sup> At this point all horizontally polarized light (logical 0) has been fil-

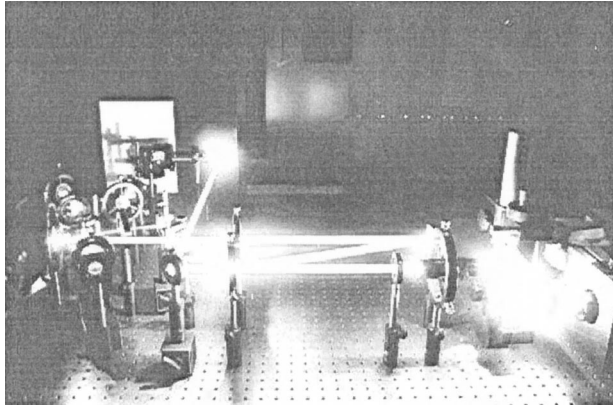


Fig. 5. The MW-OCAPP's equality demonstration system.

tered from each of the waveguides. This single-mode TM-polarized light for each word must now be coupled into a single waveguide that performs the logical OR. A single-mode Y coupler has an inherent power loss of 3 dB.<sup>29</sup> One way to circumvent these power losses is to couple into a multimode guide where insertion losses are far less. However, making the waveguide multimodal for TM light would involve increasing the height of the guide. This is undesirable because it increases the complexity of the design and would cause other coupling difficulties at the detector. Therefore a waveguide that is multimodal for TE light is chosen, such as that illustrated in Fig. 6, and a series of electro-optic modulators are required for converting the TM-polarized light to TE-polarized light.

Following coupling into the multimode waveguides, the light is separated into individual wavelengths with a vertical-walled waveguide grating spectrometer.<sup>30</sup> A 2-mm-long device provides adequate separation for 32 channels at the wavelength range of interest. These individual channels are coupled into multimode waveguides that route the light to integrated photodetectors. The photodetectors used are vertically coupled p-i-n diodes,<sup>31</sup> as shown in Fig. 7 with a matching buffer layer.<sup>32</sup> As in the bulk MW-OCAPP system, the photodetectors record the components of the ER vector.

Decoding this ER light plane is fairly simple. The light plane is a two-dimensional representation of the intersection of the CA and the RA. If  $n$  represents the number of tuples in the CA and  $m$  represents the number of tuples in the RA, then the ER must consist of

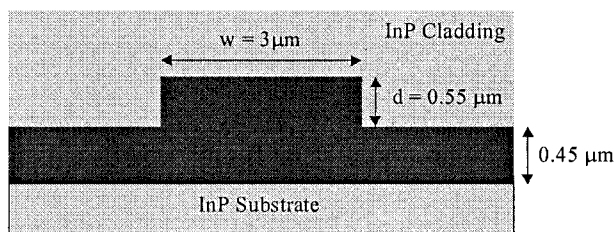
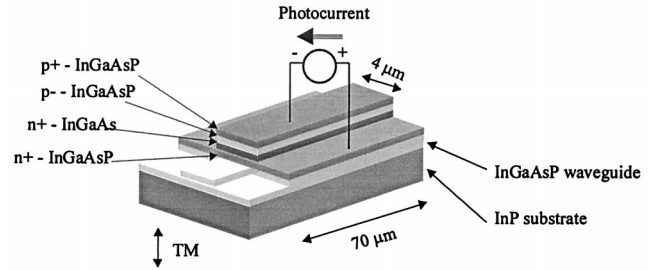
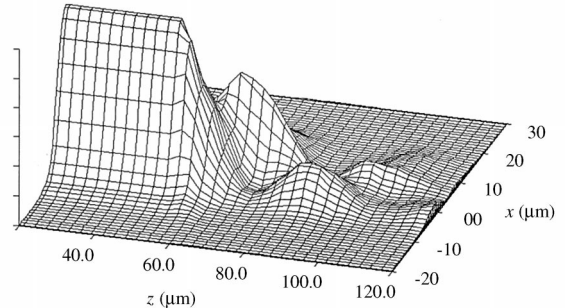


Fig. 6. Multimode waveguide cross section. Core material, InGaAsP.



(a)



(b)

Fig. 7. (a) Schematic of the integrated p-i-n photodetector. (b) The optical intensity as the light propagates through the device (Prometheus simulation).

$m \times n$  pixels. It is encoded in negative logic, meaning that nonilluminated pixels correspond to exact matches. For an  $m \times n$  ER grid, pixel <sub>$m$  $n$</sub>  is illuminated such that tuple  $RA_m$  is not equal to tuple  $CA_n$ .

The proposed system schematic for the EP<sup>3</sup>IC is illustrated in Fig. 8. This configuration has an approximate footprint of 0.32 cm  $\times$  0.32 cm.

Figure 9 illustrates the generalized method by which the EP<sup>3</sup>IC can be extended, given  $m$  CA words,  $q$  RA words, and  $n$  bits/word.

#### 4. Equivalency-Processing Parallel Photonic Integrated Circuit Performance Analysis

For evaluating whether the EP<sup>3</sup>IC system will function properly a power analysis can be performed. The analysis starts at the detector and works backward along the beam path through the waveguide components, ending ultimately at the source.

Each of the photodetectors requires  $\sim 1 \mu\text{W}$  of optical power for maintaining a signal-to-noise ratio (SNR) of 2 (Fig. 10). Therefore  $1 \mu\text{W}$  is the minimum amount of power that is to remain after all the system losses are taken into account. Each of these losses is computed in Table 1 for a design that uses 32 words in the CA, 8 words in the RA, and 32 bits/word. One can see that there is a  $-39.4\text{-dB}$  drop in power that is caused by the EP<sup>3</sup>IC's various components. An input optical power of 10 mW is reduced to  $1.2 \mu\text{W}$  by the time it reaches the detector. This level is sufficient to produce a SNR of  $\sim 3$  at the detector. The external quantum efficiency of the sources is  $\sim 38\%$ , which means that each laser source will re-

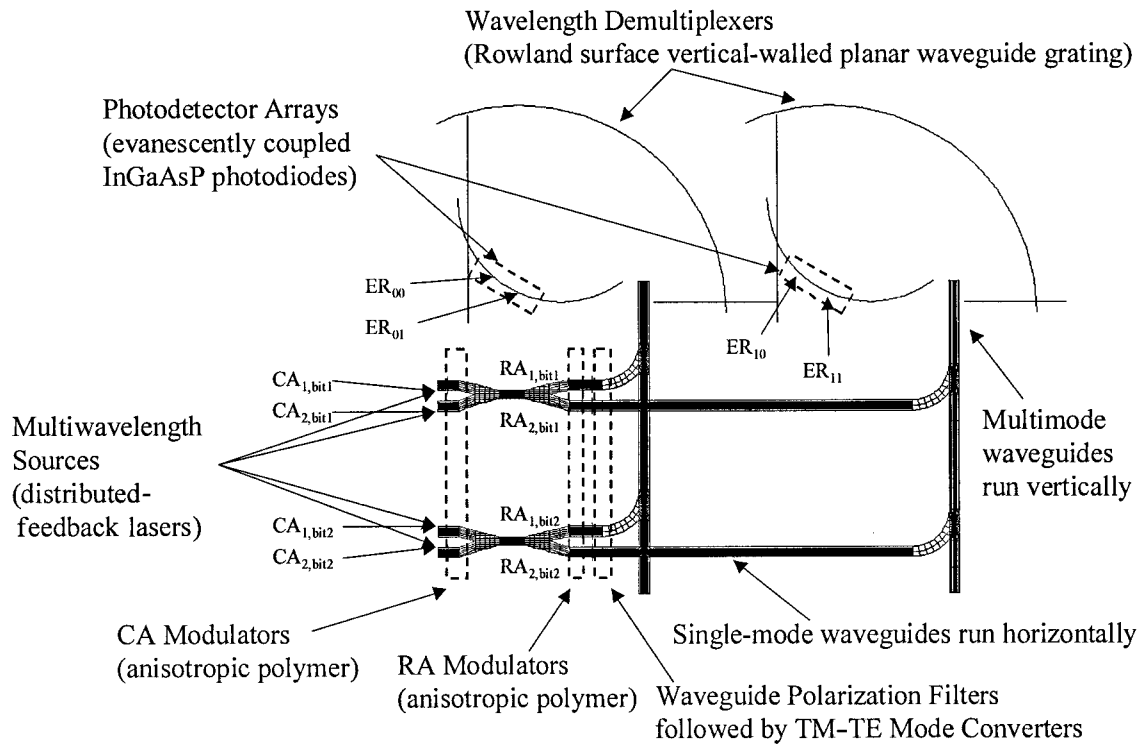


Fig. 8. EP<sup>3</sup>IC layout for a configuration consisting of two RA words, two CA words, and 2 bits/word (ASAP model).

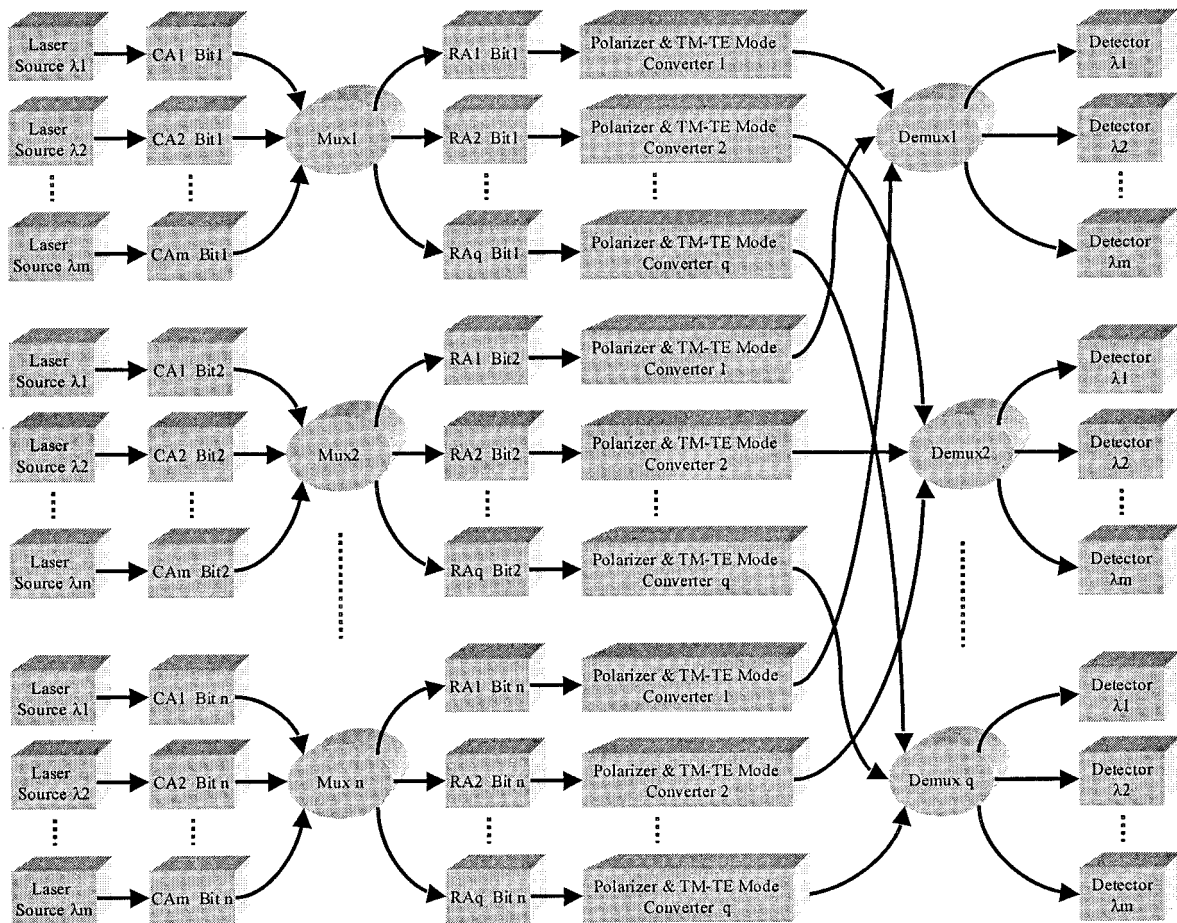


Fig. 9. Functional layout of EP<sup>3</sup>IC's generalized monolithic equality-processing core, given  $m$  CA words,  $q$  RA words, and  $n$  bits/word. Mux, multiplexer; Demux, demultiplexer.

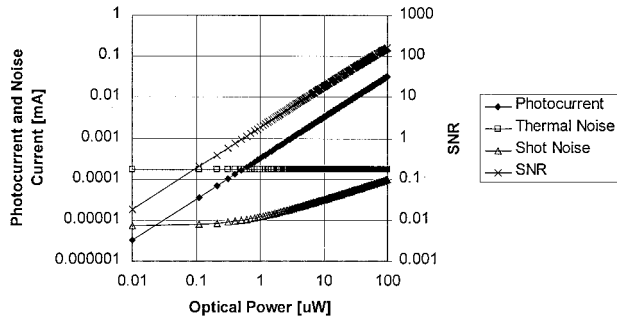


Fig. 10. Analytically derived SNR, photocurrent, and noise currents as functions of the incident optical power. A minimum SNR of 2 requires a power of  $1 \mu\text{W}$  at the photodetector.

quire  $26.3 \text{ mW}$  of input electrical power to deliver  $10 \text{ mW}$  of output optical power. The total electrical power required for all lasers is simply the product of the power per laser, the number of words in the CA, and the number of bits per word, or  $26.9 \text{ W}$ . All other sources of power consumption are insignificant when compared with the laser sources, so the average electrical power consumption for this configuration of the EP<sup>3</sup>IC is  $\sim 27 \text{ W}$ . The peak bit-comparison rate of the proposed example system is approximately  $82 \text{ Tbits/s}$ . In contrast, although the MW-CAPP is algorithmically identical to the EP<sup>3</sup>IC, its slower modulators ( $3 \text{ kHz}$ ) permit a peak bit-comparison rate of only  $24.6 \text{ Mbits/s}$  for a similarly configured machine. The footprint for this configuration of the EP<sup>3</sup>IC is approximately  $0.8 \text{ cm}^2$ .

The power-drop loss in the system is a strong function of the number of words in the RA owing to the high fan-out losses. For example, an electrical input power of  $7.9 \text{ kW/laser}$  is necessary for realizing a system with a RA word length of 64, a CA word length of 32, and a bit length of 32. This is, of course, both impractical from a power-supply standpoint and impossible from a device-integrity standpoint. Segmentation of the design into separate chips would alleviate these interconnect losses. In this approach each chip would have a RA word length of no more than 32. An electronic host would concatenate the results from each of the chips in much the same way as a single-instruction-multiple-data parallel machine operates.

We can estimate the bit-error rate (BER) for the EP<sup>3</sup>IC by referring to Fig. 10. If we assume that a SNR value of 2 corresponds to a digital 1 and that a SNR of 1 corresponds to a 0, the corresponding optical powers can be read from the plot. A digital 1 is  $\sim 1 \mu\text{W}$ , and a 0 is  $\sim 0.7 \mu\text{W}$ . For this design running at  $10 \text{ GHz}$  the computed BER per detector is  $3.6 \times 10^{-11}$ . The total BER, when we take all detectors ( $32 \times 8$ ) into account, is  $9.2 \times 10^{-9}$ . However, because the EP<sup>3</sup>IC's word-comparison rate is of the order of  $2.6 \times 10^{12}/\text{s}$ , there would be more than 92 word-comparison errors per s at the detector. Clearly, error correction would be necessary in this case. Reducing the operating frequency to  $5 \text{ GHz}$  or increasing the power per source to  $11.4 \text{ mW}$  causes the BER per detector to drop to  $7 \times 10^{-20}$ . The

Table 1. Worst-Case Power Loss Analysis

Description	Expression	Value
Number of words in the CA plane	$a$	32
Number of words in the RA plane	$b$	8
Number of bits/word	$c$	32
Modulator loss	—	-0.1 dB
Number of Y-coupler junctions	$\log_2(a)$	5
Loss per single-mode junction	—	-3 dB
Total loss	—	-15 dB
Number of Y-splitter junctions	$\log_2(b)$	3
Loss per junction	—	-0.195 dB
Total loss	—	-0.585 dB
Number of fan-out guides	$b$	8
Fan-out power drop per guide	$10 \times \log_{10}(1/b)$	-9.03 dB
Modulator loss	—	-0.1 dB
Polarization filter loss	—	-2 dB
Modulator loss	—	-0.1 dB
Number of $t$ crossings (horizontal)	$b - 1$	7
Power drop per $t$ crossing	—	-0.025 dB
Total drop for $t$ crossings	—	-0.175 dB
Waveguide bend loss	—	-0.05 dB
Y-coupler single-mode insertion loss	—	-1.43 dB
Number of Y-coupler multimode crossings	$c - 1$	31
Multimode insertion loss per coupler	—	-0.056 dB
Total Y-coupler loss	—	-1.736 dB
Number of $t$ crossings (vertical)	$(b - 1) \times c$	224
Power loss per $t$ crossing	—	-0.025 dB
Total loss	—	-5.6 dB
Demultiplexer diffraction loss	—	-3 dB
Detector loss	—	-0.5 dB
Single-laser power output	$d$	10 mW
Total source optical power	$a \times c \times d$	10.24 W
Total loss	$e = \Sigma(\text{losses})$	-39.37 dB
Power fraction available to a photodetector	$f = 10^{(e/10)}$	0.000116
Power available to a photodetector	$d \times f$	$1.2 \mu\text{W}$

aggregate error rate for all detectors is then  $1.79 \times 10^{-17}$ . The number of word-comparison errors per second is a mere  $9.1 \times 10^{-8}$  at 5-GHz operation.

A major obstacle that may hamper the EP<sup>3</sup>IC's high-speed processing potential is in the communication link with the electronic host system. The current state of the art in commercial electrical peripheral bus speed is approximately  $400 \text{ MHz}$ .<sup>33</sup> The aggregate input-output (I/O) transfer rate with a 64-bit-wide bus is  $25.6 \text{ Gbits/s}$ . Although fast by today's computing standards, this rate pales in comparison with the EP<sup>3</sup>IC's communication I/O bandwidth requirements of  $15.4 \text{ Tbits/s}$  ( $12.8 \text{ Tbits/s}$  input and  $2.6 \text{ Tbits/s}$  output). Obviously there would be a severe I/O bottleneck if an electrical bus were used. To eliminate the bottleneck would require for the equivalent electrical bus an impossible

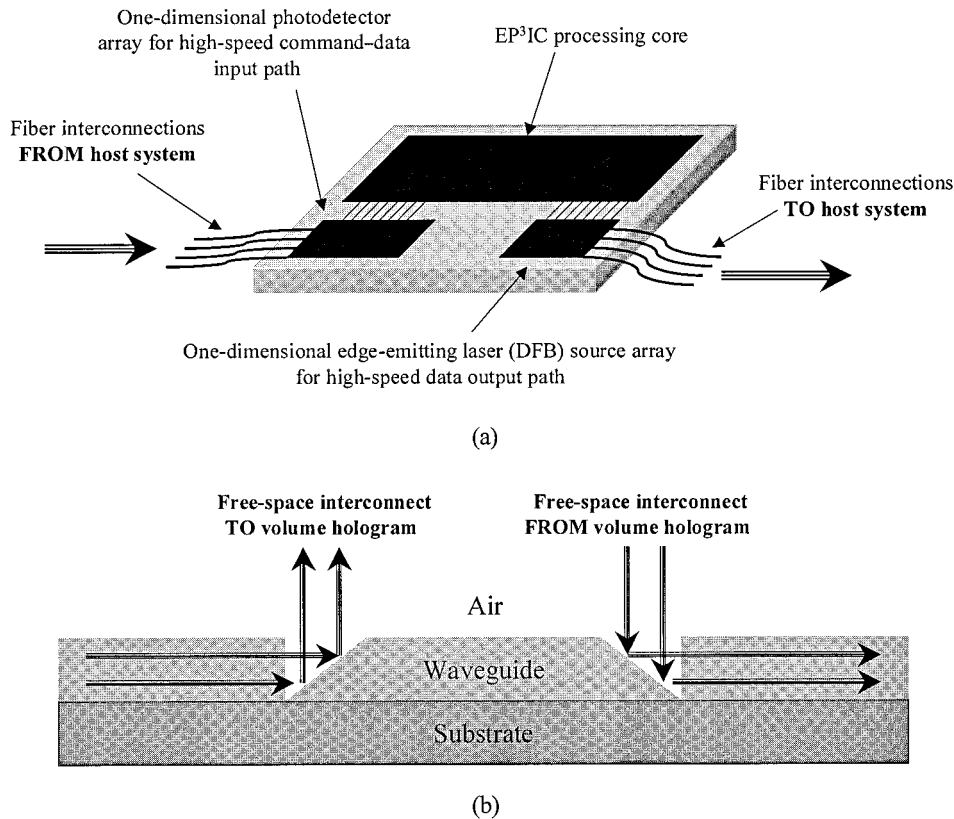


Fig. 11. (a) Proposed interchip I/O communication layout with fiber interconnects. (b) A waveguide mirror coupler could be used to realize free-space optical interconnects between the EP<sup>3</sup>IC processor and other components. This setup is ideally suited for high-speed parallel interfacing with optical memory, such as in a page-oriented volume hologram.

width of 38,500 bits! A higher-bandwidth interconnection fabric is required: optical interconnects.

Given an optical modulation rate of 10 GHz, an optical bus width of 1540 bits (1 bit/fiber) would be required for alleviating the bottleneck. Signal multiplexing with multiple wavelengths can further reduce the number of fibers required. If 10 wavelengths (each modulated by a separate channel) are multiplexed per fiber, the number of required fibers reduces to 154.

Figure 11(a) illustrates the proposed interchip communications layout. The primary link consists of fiber interconnections that are butt coupled to a linear source and detector arrays at the cleaved edges of the EP<sup>3</sup>IC substrate. This approach requires no significant device additions to the manufacturing process because planar sources, a waveguide, and detectors are already present and optimized within the EP<sup>3</sup>IC architecture.

Interfacing the EP<sup>3</sup>IC with page-oriented holographic memory for purely optical input and output is made possible by use of waveguide mirror couplers,<sup>34</sup> such as are illustrated in Fig. 11(b). The 45°-angled facets permit light to be coupled into and out of the planar waveguide from normal incidence. It is conceivable that a two-dimensional array of such couplers could be arranged on the EP<sup>3</sup>IC substrate to facilitate parallel interfacing with an optical memory

Table 2. EP<sup>3</sup>IC Performance Summary

Description	Value
Device footprint	0.8 cm <sup>2</sup>
Material system	InP
Electrical power consumption (processor)	27 W
Peak bit-comparison rate	82 Tbits/s
Input bandwidth requirement	12.8 Tbits/s
Output bandwidth requirement	2.6 Tbits/s
Laser source operation range	1.40–1.65 μm
System BER	1.2 × 10 <sup>-9</sup>

device. Table 2 lists a summary of the EP<sup>3</sup>IC's performance parameters for a system consisting of 32 CA words, 8 RA words, and a word length of 32 bits.

## 5. Conclusions

In this paper we have presented an architectural design called the EP<sup>3</sup>IC that combines the superior optical parallelism present in the MW-OCAPP with the processing speed and the manufacturability that are allowed for by photonic integrated circuits. The proposed configuration of the EP<sup>3</sup>IC (32 comparand words, 8 database words, and 8 bits/word) has a theoretical peak bit-comparison rate of 82 Tbits/s and an average electrical power consumption of 27 W. Ongoing project research includes the incorporation of logic devices into the EP<sup>3</sup>IC to facilitate I/O and con-



trol operations. Additional efforts include an investigation into the integration of higher-order database operations as well as the seeking out of additional applications that would be suitable for an EP<sup>3</sup>IC-like device. Device fabrication and prototyping is, in addition, under investigation.

This research was supported by National Science Foundation grant MIP-9505872.

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