Call for Papers

HPCRI: 3rd Workshop on High Performance Computing
Reliability Issues

To be held in conjunction with
the 13th International Symposium on High Performance Computer Architecture
(HPCA-13)
February 10-14, 2007

Application demands and trends in the hardware and software industry have necessitated the development of High Performance Computing Systems with high availability and reliability. Clusters and grids are a cost-effective way of solving high performance computing needs and are built by using thousands of commodity systems that are geographically distributed and provide fast, dependable and reliable access to data and resources. Thus reliability of the underlying platform is essential to high performance computing. The design trends in the circuit technology with smaller die sizes and faster clock speeds have made the components more prone to random errors and crosstalk. Fault tolerant approaches in the hardware/micro architecture are necessary to mitigate component level errors.

This workshop provides a forum for discussing current research and practices in error management in high performance computing systems. Participants from industry and academia address the reliability and availability needs for HPC and the integration of hardware and software techniques into enterprise server systems to ensure continues availability. Recent developments and future direction will be presented in order to share and stimulate ideas for developing highly reliable systems for performing high performance tasks. The workshop will have several areas of focus: trends in rates of errors and types of errors, error detection and recovery mechanisms, fault prediction, and fault-driven provisioning of large scale systems.

**Topics of interest include (but are not limited to):**

- Error Detection, Mitigation and Recovery
  - Error Types and Rates
  - Characterization of Errors (e.g., radiation-induced, hard, intermittent, etc.)
  - Detection Mechanisms
  - Monitoring Tools and Techniques
  - Error Detection Latencies
  - Performance Impacts / Overhead
  - Techniques for Error Recovery
- Reliability Design
  - Caches/memory architecture
  - Interconnect architecture
- Fault Prediction
- Fault Modeling
- Self-healing / Autonomics for error handling in cluster/grid environments
- Hardware Redundancy Techniques to decrease error rates
- Case studies discussing the engineering tradeoffs in providing automated fault management in HPC systems
**Paper Submission Information:**

We welcome submissions in the form of abstracts (< 1 page) and short papers (5-7 pages). Submissions that describe ongoing research in the above areas are encouraged. Please e-mail your submissions (preferably in pdf) to padmashree.k.apparao@intel.com, (kalbar@crhc.uiuc.edu), and gregory.s.averill@intel.com

**Workshop Chairs:**

Padma Apparao  Intel Labs  padmashree.k.apparao@intel.com
Zbigniew Kalbarczyk  University of Illinois at Urbana Champaign  kalbar@crhc.uiuc.edu
Greg Averill  Intel Labs  gregory.s.averill@intel.com

**Organizing / Program Committee:**

Wen-mei Hwu  University of Illinois at Urbana Champaign
Subhasish Mitra  Stanford University
Giacinto Paolo Saggese  Nvidia
Fabrizio Petrini  Pacific Northwest National Labs
Joseph Torrellas  University of Illinois at Urbana Champaign
Timothy Tsai  Sun Microsystems

**Important Dates:**

- **Abstract Submission:** November 1, 2006
- **Paper Submission:** November 21, 2006
- **Notification of Acceptance:** December 6, 2006
- **Camera-ready due:** January 15, 2007

**Workshop Activities:**

Workshop activities will include a keynote, an invited papers’ session and peer-reviewed technical sessions.

**Workshop Publication:**

We will distribute published proceedings at the workshop.

For further details on the workshop and any questions please contact Padma Apparao (padmashree.k.apparao@intel.com) or Zbigniew (kalbar@crhc.uiuc.edu) or Greg Averill (gregory.s.averill@intel.com).