## Technical Program Schedule

### Saturday, February 10th, 2007

| All Day Events | Workshop RIDMS-2: Second Workshop on Real-Time and Interactive Digital Media Supercomputing |

### Sunday, February 11th, 2007

| All Day Events | Workshop INTERACT-11: Eleventh Workshop on Interaction between Compilers and Computer Architectures  
Workshop CAECW-10: Tenth Workshop on Computer Architecture Evaluation using Commercial Workloads |
| Morning Events | Workshop RIDMS-2: Second Workshop on Real-Time and Interactive Digital Media Supercomputing  
Workshop CMP-MSI: First Workshop on Chip Multiprocessor Memory Systems and Interconnects  
Tutorial: Practical Cache Performance Modeling for Computer Architects  
Y. Solihin (NCSU), T. Puzak, and P. Emma (IBM Research) |
| Afternoon Events | Workshop CARD: First Workshop on Computer Architecture Research Directions  
Tutorial: Microprocessor Memory Array Circuits for Architects |
|                 | 6:00PM - 8:00PM | HPCA Conference Reception |

### Monday, February 12th, 2007

| 7:30AM - 8:30AM | Breakfast |
| 8:30AM - 8:50AM | Welcome Message |
| 8:50AM - 10:00AM | Keynote I  
Interconnect-Centric Computing  
Bill Dally (Willard R. and Inez Kerr Bell Professor of Engineering and Chairman, Department of Computer Science, Stanford University)  
Abstract: As we enter the many-core era, the interconnection networks of a computer system, rather than the processor or memory modules, will dominate its performance. Several recent developments in interconnection network architecture including global adaptive routing, high-radix routers, and technology-matched topologies offer large improvements in the performance and efficiency of this critical component. The implementation of a portion of several interconnection networks on multi-core chips also raises new opportunities and challenges for network design. This talk explores the role of interconnection networks in modern computer systems, recent developments in network architecture and design, and the challenges of on-chip interconnection networks. Examples will be drawn from several systems including the Cray BlackWidow. |
| 10:00AM - 10:30AM | Break |
| 10:30AM - 12:00PM | Session 1: Multiprocessor Architectures  
An Adaptive Shared/Private NUCA Cache Partitioning Scheme for Chip Multiprocessors  
H. Dybdahl (Norwegian University of Science and Technology) and P. Stenström (Chalmers)  
Evaluating MapReduce for Multicore and Multiprocessor Systems  
C. Ranger, R. Raghuraman, A. Penmetta, G. Bradski and C. Kozyrakis (Stanford University)  
Extending Multicore Architectures to Exploit Hybrid Parallelism in Single-Thread Applications |
<table>
<thead>
<tr>
<th>Time</th>
<th>Session</th>
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<tbody>
<tr>
<td>12:00PM - 1:30PM</td>
<td>Lunch</td>
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<tr>
<td>1:30PM - 3:00PM</td>
<td>Implications of Device Timing Variability on Full Chip Timing</td>
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<td></td>
<td>M. Annavaram, E. Grochowski, and P. Reed (Intel)</td>
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<td></td>
<td>Optical Interconnect Opportunities for Future Server Memory Systems</td>
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<tr>
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<td>Y. Katayama and A. Okazaki (IBM)</td>
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<td>3:00PM - 3:30PM</td>
<td>Break</td>
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<td>3:30PM - 5:00PM</td>
<td>Feedback Directed Prefetching: Improving the Performance and</td>
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<td>Bandwidth-Efficiency of</td>
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<td>Hardware Prefetchers</td>
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<td></td>
<td>S. Srinath (Microsoft and The University of Texas at Austin), O. Mutlu</td>
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<td></td>
<td>(Microsoft Research), H. Kim, and Y. Patt (University of Texas at</td>
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<td>Austin)</td>
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<td></td>
<td>Improving Branch Prediction and Predicated Execution in Out-of-Order</td>
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<td>Processors</td>
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<td></td>
<td>E. Quiñones, J.M. Parcerisa (Universitat Politècnica de Catalunya)</td>
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<td></td>
<td>and A. González (Intel and Universitat Politècnica de Catalunya)</td>
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<td></td>
<td>Accelerating and Adapting Precomputation Threads for Efficient</td>
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<td>Prefetching</td>
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<td>W. Zhang, B. Calder, and D. Tullsen (University of California, San</td>
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<td>Diego)</td>
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<td>6:00PM - 7:30PM</td>
<td>TCC Business Meeting</td>
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**Tuesday, February 13th, 2007**

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<th>Time</th>
<th>Session</th>
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<tr>
<td>7:30AM - 8:30AM</td>
<td>Keynote II</td>
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<tr>
<td></td>
<td>Petascale Computing Research Challenges – A Manycore Perspective</td>
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<td></td>
<td>Steve Pawlowski (Senior Fellow and Chief Technology Officer of</td>
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<td>the Digital Enterprise Group, Intel Corporation)</td>
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<tr>
<td></td>
<td>Abstract: Future High Performance Computing will undoubtedly reach</td>
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<td>Petascale and beyond. Today’s HPC is tomorrow’s Personal Computing.</td>
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<td>What are the evolving processor architectures towards Multi-core and</td>
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<td>Many-core for the best performance per watt; memory bandwidth</td>
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<td>solutions to feed the ever more powerful processors; intra-chip</td>
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<td>interconnect options for optimal bandwidth vs. power? With Moore’s</td>
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<td>Law continuing to prove its viability and shrinking transistors’</td>
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<td>geometry mean that improving reliability is even more challenging.</td>
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<td>Intel Senior Fellow and Chief Technology Officer of Intel’s Digital</td>
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<td>Enterprise Group, Steve Pawlowski, will provide his technology vision,</td>
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<td>insight and research challenges to achieve the vision of Petascale</td>
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<td>computing and beyond.</td>
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<td>9:30AM - 10:00AM</td>
<td>Break</td>
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<td>10:00AM - 12:00PM</td>
<td>Session 4: Memory Systems I (Parallel Session)</td>
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<td></td>
<td>A Scalable, Non-blocking Approach to Transactional Memory</td>
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<td></td>
<td>H. Chaﬁ, J. Casper, B. Carlstrom, A. McDonald, C. Cao Minh, W. Baek,</td>
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<td>K. Kozyrakis, and K. Olukotun (Stanford University)</td>
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<td>Fully-Buffered DIMM Memory Architectures: Understanding</td>
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<td>Mechanisms, Over-heads and Scaling</td>
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<td>B. Ganesh, B. Jacob (University of Maryland College Park), D. Wang</td>
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<td>(Metaram), and A. Jaeeel (Intel)</td>
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<td>HARD: Hardware-Assisted Lockset-Based Race Detection</td>
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<td>P. Zhou, R. Teodorescu, and Y. Zhou (University of Illinois at</td>
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<td>Urbana-Champaign)</td>
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<td>Colorama: Architectural Support for Data-Centric Synchronization</td>
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<td>L. Ceze, Pablo Montesinos (University of Illinois at Urbana-Champaign),</td>
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<td>C. von Praun (IBM T J Watson) and J. Torrellas (University of Illinois</td>
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<td>at Urbana-Champaign)</td>
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<td>10:00AM - 12:00PM</td>
<td>Session 5: Error Detection and Fault-Tolerance (Parallel Session)</td>
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<td>Error Detection Via Online Checking of Cache Coherence with Token</td>
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<td>Coherence Signatures</td>
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<td>A. Meixner and D. Sorin (Duke University)</td>
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<td>A Low Overhead Fault Tolerant Coherence Protocol for CMP Architectures</td>
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<td>R. Fernández-Pascual, J. García, M. Acacio, and J. Duato, (Universidad</td>
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<td>de Murcia and Universidad Politécnica de Valencia)</td>
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<td>Perturbation-Based Fault Screening</td>
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<td>P. Racunas (Intel), K. Constantinides (University of Michigan), S.</td>
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<td>Manne, and S. Mukhejee (Intel)</td>
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### Session 6: Thermal Modeling and SIMD (Parallel Session)

**Thermal Herding: Microarchitecture Techniques for Controlling HotSpots in High-Performance 3D-Integrated Processors**
K. Puttaswamy and G. Loh (Georgia Institute of Technology)

**Modeling and Managing Thermal Profiles of Rack-Mounted Servers with ThermoStat**
J. Choi, Y. Kim, A. Sivasubramaniam, J. Srebric, Q. Wang (Pennsylvania State University), and J. Lee (KAIST)

**Liquid SIMD: Abstracting SIMD Hardware Using Lightweight Dynamic Mapping**
N. Clark, A. Hormati, S. Mahlke (University of Michigan), S. Yehia, and K. Flautner (ARM)

### Session 7: Chip Multiprocessors, Simultaneous Multi-threading, and Caches (Parallel Session)

**Interactions Between Compression and Prefetching in Chip Multiprocessors**
A. Alameldeen (Intel) and D. Wood (University of Wisconsin-Madison)

**A Memory-Level Parallelism Aware Fetch Policy for SMT Processors**
S. Eyerman and L. Eeckhout (Ghent University)

**Line Distillation: Increasing Cache Capacity By Filtering Unused Words in Cache Lines**
M. Qureshi, M. Suleman, and Y. Patt (University of Texas at Austin)

### Panel

**Researching Novel Systems: To Instantiate, Emulate, Simulate, or Analyticate?**
**Moderator:** Doug Burger (University of Texas at Austin)

**Panel Members:**
- Joel Emer (Intel)
- Phil Emma (IBM)
- Steve Keckler (University of Texas at Austin)
- Yale Patt (University of Texas at Austin)
- Dave Patterson (University of California, Berkeley)

**Description:** The computer architecture research community has a rich menu of methodological options, which includes building full system prototypes, measuring in simulation, emulating on FPGAs, or constructing sophisticated analytic models. However, building custom systems has become enormously expensive, especially given the current funding climate. Simulations have become enormously complex as well, often including full operating systems. Analytic models have become less popular as system complexity has grown. Finally, some argue that FPGA emulation of hardware is the right approach for the future, while others opine that it is the worst of all worlds. This panel will debate these various points of view, which are of great interest to the funding sponsors of our community.

### Banquet

**Wednesday, February 14th, 2007**

**7:00AM - 8:00AM**
**Breakfast**

**8:00AM - 10:00AM**

**Session 8: Memory Systems II**

**LogTM SE: Decoupling Hardware Transactional Memory from Caches**

**MemTracker: Efficient and Programmable Support for Memory Access Monitoring and Debugging**
G. Venkataramani, B. Roemer (Georgia Institute of Technology), Y. Solihin (North Carolina State University) and M. Prvulovic (Georgia Institute of Technology)

**A Burst Scheduling Access Reordering Mechanism**
J. Shao and B. Davis, (Michigan Technological University)

**Exploiting Postdominance for Speculative Parallelization**
M. Agarwal, K. Malik, K. Woley, S. Stone, M. Frank (University of Illinois at Urbana Champaign)

**10:00AM - 10:30AM**
**Break**
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<tr>
<th>Time</th>
<th>Session 9: Virtual Machines, Caches and Modeling</th>
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| 10:30AM - 12:30PM | **Concurrent Direct Network Access for Virtual Machine Monitors**  
P. Willmann, J. Shafer, D. Carr (Rice University), A. Menon (EPFL), S. Rixner, A. Cox (Rice University), and W. Zwaenepoel (EPFL)  
**A Domain-Specific On-Chip Network Design for Large Scale Cache Systems**  
Y. Jin, E. Kim (Texas A&M University), K. Yum (University of Texas, San Antonio)  
**An Adaptive Cache Coherence Protocol Optimized for Producer-Consumer Sharing**  
L. Cheng, J. Carter (University of Utah), and D. Dai (SGI)  
**Illustrative Design Space Studies with Microarchitectural Regression Models**  
B. Lee and D. Brooks (Harvard University) |
| 12:30PM      | **Conference Program Ends**                                                                                   |