Signal Integrity in Digital Systems

**Objective:** Basics signal integrity concepts

**Outline:**
1. Circuit attributes for signal integrity
2. Electrical systems
3. Interconnect modeling
4. Modeling criteria
1. Circuits attributes for signal integrity

LOGIC SWING, RISE AND FALL TIMES, CYCLE TIME
Logic swing

\[ V_{LS} = V_H - V_L = \begin{cases} 5 \text{volts} & \text{CMOS} \\ 3.3 \text{volts} & \text{BJT} \\ 0.8 \text{volts} & \end{cases} \]

Rise time - \( t_r \), Fall time - \( t_f \)

\[ t_r = t_f = \begin{cases} 100 - 500 \, \text{ps} & \text{CMOS} \\ 80 - 200 \, \text{ps} & \text{BJT} \end{cases} \]

Cycle time – \( T_c \)
Estimation of Highest Frequency of Interest Using Rise Time

Fundamental frequency

\[ \nu_o = \frac{1}{T_c} \]

Taking 3-td harmonic as highest frequency to be transmitted

\[ f_{\text{max}} = \frac{3}{T_c} \]

A simplified relation the rise time and cycle time

\[ T_c = 10t_r \]

yields

\[ f_{\text{max}} = \frac{0.3}{T_c} \cdot \]

Example: \( t_r = 100[\mu\text{sec}] \) \( \Rightarrow \)

\[ f_{\text{max}} = \frac{0.3}{100 \cdot 10^{-12}} = 3[\text{GHz}] \]
Characterization of logic circuits (terminal properties)

Static: transfer curve (transfer characteristic)

The transfer curve is used to determine

logic swing
switching threshold
noise tolerances
noise margins
noise immunities
A prototypical transfer curve (steady state response)

$NT_{H(L)}$ - noise tolerance (sensitivity); $NM_{H(L)}$ - noise margin

Noise immunity ($NI$): $NI_{H(L)} = \frac{NT_{H(L)}}{V_{LS}}$
Dynamic characterization

Transient response:

\( V_{IN} \) and \( V_{OUT} \) are transitioning between "high" and "low" levels

yielding:

a) gate delay (internal delay)

b) dynamic noise tolerance
a) Definition of gate delay, \( t_D \), (aka internal delay)

\[
V_{IN}^L + \frac{1}{2} V_{LS}^{IN} \quad t_{D1} \quad t_{D2} \\
V_{OUT}^L + \frac{1}{2} V_{LS}^{OUT}
\]

\[
t_D = \frac{1}{2} (t_{D1} + t_{D2})
\]
b) Dynamic noise tolerance (DNT)

The DNT curves are generated using circuit simulation with perturbing pulses added to the input signal. The DNT are determined via receiver characterization or circuit simulation.
Dynamic characterization of logic circuits

Dynamic noise tolerance  ⇒  for receivers

Driving capability  ⇒  for drivers

determined through study of **driver-line interaction** via

circuit simulation
characterization

**Driver power (current) demand** (needed for estimation of switching perturbations) - determined via

circuit simulation
characterization
2. Electrical Systems

1. Signal distribution system

   Problems:
   - signal delay
   - signal distortion via
     - coupling noise
     - switching noise
     - reflections
   - losses (causing attenuation and dispersion)

2. Power and ground distribution system

   Problems:
   - DC voltage drop
   - switching noise

3. Externally coupled systems:  
   - E-M Interference (EMI)
   - Electro-static discharge (ESD)
3. Interconnect Modeling

Signal interconnections

- finite impedance \((40-70 \ \Omega)\)
- low currents
- components

  *traces on-chip and bonds (WB, TAB, FC)*
  *conductors on chip carriers and connections (pins, SMT, balls)*
  *PWB conductors*
  *connectors*

Power and ground connections

- very low impedance \((m\Omega, \mu\Omega)\) - lower than better
- higher currents \((mA, A)\)
- components

  *traces on-chip and bonds*
  *conducting plates in packages and boards*
Remarks concerning on-chip interconnections

**Modeling:** propagation modes

**Coupling:**
- capacitive
- inductive

**Technological trends - effects of scaling**
- increased capacitive coupling
- increased importance of process variations
- decreased noise immunity
- decreased reliability (electromigration), yield (contamination effects)
Magnetic field strength (and the flux) is proportional to loop current.
A fraction of the magnetic flux from the loop A encompasses the loop B.
Voltage induced in the loop B is proportional to the rate of change of flux in the loop A.
Ground planes keep the loops small and local thus reducing inductive coupling.
Inductive coupling reaches farther (encompasses more conductors) than capacitive coupling, which typically is more localized and decays rapidly with the distance.
Effect of backplane

Removed ground plane

Ground (backplane) included

The resistive losses in the substrate are approximated by

$$\tan(\delta) = \frac{1}{\omega \varepsilon_r \varepsilon_0 \rho}$$

Depending on frequency and resistivity the substrate may behave as a conductor or a dielectric and may determine various signal propagation modes yielding various velocities of signal propagation.
Results of approximate analysis

Idealized structure

Graphical representation of results

Example for:  \( b_1 = 1 \mu m, b_2 = 400 \mu m \)
(Grabinski, 1991).
Capacitive coupling is important

Example of prototypical results for fixed distance to the ground ($\approx 2\mu m$)

![Graph]

- $C_G$ - capacitance to the ground
- $C_c$ - coupling capacitance (to the neighbor)
- $C_t$ - total capacitance
Trends

Increasing number of layers is needed due to chip complexity.

Lines are longer and require higher aspect ratio to cope with space and attenuation restriction - consequently they exhibit more crosstalk.

Processing variations are more important because lines are very tight and narrower.

Hierarchical wiring is needed: RC models for lower levels, TL for higher levels.

Skin effect might be important on higher level interconnects

\[
\delta = \sqrt{\frac{2}{\omega \rho \mu}}; \quad \sigma \approx 2 \mu m \quad \text{for copper at 1 GHz.}
\]
Example of effects caused by interconnect geometry scaling by a factor of 2 and a reduction of supply voltage from 2.5 [V] to 1.8 [V].

**Geometry**

Base technology: \( W = 0.9 \mu m \), \( S = 0.9 \mu m \), \( T = 0.9 \mu m \), \( k_c = 0.53 \)

Scaled technology: \( W = 0.45 \mu m \), \( S = 0.45 \mu m \), \( T = 0.73 \mu m \), \( k_c = 0.72 \).

**Typical circuit noise immunity:**

Base technology: \( \frac{(650 - 1500)[mV]}{2.5[V]} \) yields \((24 - 60)\% \) of \( V_{DD} \)

Scaled technology: \( \frac{(650 - 1000)[mV]}{1.8[V]} \) yields \((36 - 56)\% \) of \( V_{DD} \).

**Typical relative signal coupled noise**

Base technology: \( \frac{(500 - 700)[mV]}{2.5[V]} \) yields \((20 - 28)\% \) of \( V_{DD} \)

Scaled technology: \( \frac{(700 - 800)[mV]}{1.8[V]} \) yields \((38 - 45)\% \) of \( V_{DD} \).
4. Modeling Criteria for Signal Interconnections
(based on single line analysis)

Schematic of a line

Basic relation used in derivation: \( \lambda = v \frac{2\pi}{\omega} \)

Frequency domain criteria are based on comparison of line length to minimum signal wavelength as determined by the higher frequency signal to be transmitted through the interconnecting line.
Simplified criteria

\[
\frac{t_r}{t_D} \geq 100 \quad \text{- ideal wire}
\]

\[
4 < \frac{t_r}{t_D} < 100 \quad \text{- lumped RC}
\]

\[
\frac{t_r}{t_D} \leq 4 \quad \text{- transmission line}
\]

Alternative criteria (rule of thumb used by some designers):

If \( t_r > 2.5t_D \) \( \rightarrow \) use lumped model

If \( t_r > 2.5t_D \) \( \rightarrow \) use transmission line model

A useful relation to estimate time of flight:

\[
t_D = D\sqrt{\ell c} = D\tau; \quad \tau \approx 33.3\sqrt{\varepsilon_r} \text{ [ps/cm]}
\]
Exercise

Determine model required for the interconnect of geometry given below

Dimensions are given in mils

Assume rise time $t_r = 100 \text{[ps]}$ and consider two cases:

a) interconnect on chip carrier where $D = 60 \text{[mils]}$

b) interconnect on a board where $D = 25 \text{[cm]}$. 