(Feb. 27, 2003, 11:00-12:15 during class)
For all problems, you can assume the following transistor parameters (unless otherwise mentioned):

**NMOS:**
\[ V_{th} = 0.4, \ k'_n = 115 \ \mu A/V^2, \ V_{DSAT} = 0.6 V, \ \lambda = 0, \ \gamma = 0.4 \ V^{1/2}, \ 2\Phi_F = -0.6 V \]

**PMOS:**
\[ V_{tp} = -0.4 V, \ k'_p = -30 \ \mu A/V^2, \ V_{DSAT} = -1 V, \ \lambda = 0, \ \gamma = -0.4 \ V^{1/2}, \ 2\Phi_F = 0.6 V \]

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Problem 1: ___ / 10
Problem 2: ___ / 15
Problem 3: ___ / 5
Total: ___ / 30
PROBLEM 1. (10 pts) MOS transistor as a switch

a) (4 pts) Find the final value of the voltage $V_o$ (the node with an arrow pointing out) as a response to a LH transition at the input as shown in Figures 1.a – 1.d. Assume $V_{TN} = |V_{TP}| = 0.5\text{V}$. Assume that the capacitor is initially discharged, and ignore subthreshold conduction and body effect.

Figure 1.a.

Figure 1.b.

Figure 1.c.

Figure 1.d.
b) (2pts) When the output reaches its final value, a 2.5V to 0 step is applied to the input. Determine the energy consumed in the transistors from Figure 1.c. during the transition (in symbolic terms).

Energy Consumed = charging of capacitor from 0 to \((V_{DD} - 2V_T)\)

\[ \int_{0}^{V_{DD} - 2V_T} C \cdot (V_{OUT}) \, dV_{OUT} \]

\[ = \frac{1}{2} C \left( V_{DD} - 2V_T \right)^2 \]
c) (6 pts) For Figure 1.d, find the energy dissipated in the transistor during the first 0→1 transition. Then, when the output reaches its final value, a 2.5V to 0 step is applied to the input, followed by the second 0 to 2.5V step. Find the energy dissipated in the transistor in the first 1→0 transition, and the second 0→1 transition (in symbolic terms).

(a) 0→1

The capacitor charges up from 0 to VDD.

In a PMOS device, the device is "On" always from 0 to VDD, so the energy dissipated is:

\[ E_{0→1} = \frac{1}{2} CV_{DD}^2 \]

(b) 1→0

The capacitor discharges from VDD to Vt.

Energy dissipated:

\[ \frac{1}{2} CV_{DD}^2 - \frac{1}{2} CV_t^2 \]

\[ = \frac{1}{2} C [V_{DD}^2 - V_t^2] \]

(c) Proceeding in the same manner, we get

First \( E_{0→1} = \frac{1}{2} CV_{DD}^2 \)

First \( E_{1→0} = \frac{1}{2} C [V_{DD}^2 - V_t^2] \)

Second \( E_{0→1} = \frac{1}{2} C [V_{DD}^2 - V_t^2] \)
Consider the following simple circuit (implemented in the 1.2 µm CMOS technology). Assume $V_{DD} = 3$ V and use the following transistor parameters: $C_{ox} = 1.75 \text{ fF/µm}^2$, $x_f$ (lateral diffusion) = 0.15 µm, $C_{j0} = 3.0 \times 10^{-4} \text{ F/m}^2$, $m_f = 0.5$, $C_{jw0} = 8.0 \times 10^{-10} \text{ F/m}$, $m_{jw} = 0.5$, $\phi_0 = 0.9$ V and $v_r = 0.4$ V.

Hint:
Use $C_o = C_{ox} x_f$ to calculate the per unit length overlapping capacitance.

Assume that $V_G$ is initially at 0 V. We want the compute the time it will take to raise $V_G$ to $V_{DD}$. To do so, we will lump the device parasitic capacitances into a single lumped capacitance. This capacitance is a function of the operation region of the device.

a. Determine the operation regions the MOS transistor is traversing during the transient (for $V_G$ going from 0 to $V_{DD}$).

Region 1: Saturation
Region 2: Cutoff
Region 3: ... 

$V_{DS} = 3$ V  ->  triode region
$V_G < 0$  ->  Vas unrelated.
b. Determine the capacitance seen at the gate of the MOS transistor in each of these regions.

$$C_g = C_{ox} \frac{W}{L} + 2 C_{ox} \frac{W}{W}$$

in um

$$= 1.75 \times 3 \times 12 \ \text{fF} + 2 \times 1.75 \times 0.15 \times 3$$

$$\Rightarrow 6.3 + 1.575 = 7.875 \ \text{fF}$$
\[ C_g = \frac{2}{3} \text{CoxWL} + 2 \text{CoxW} \]

\[ \Rightarrow 4.2 + 1.575 \]

\[ \Rightarrow 5.775 \text{fF} \]

\[
\begin{array}{|c|c|}
\hline
\text{region 1):} & 7.875 \text{fF} \\
\text{region 2):} & 5.575 \text{fF} \\
\text{region 3):} & \\
\hline
\end{array}
\]

e Determine the total time it will take for \( V_{eq} \) to go from 0 V to \( V_{TH} \) (for \( I_m = 100 \mu A \)).

\[
I = C_g (V_{eq}) \frac{dV_{eq}}{dt}
\]

\[
I = \frac{1}{T} \int_{0}^{V_{DD}} C_g (V_{eq}) dV_{eq}
\]

\[
I = \frac{1}{T} \int_{0}^{V_T} C_g \text{cut} dV_{eq} + \int_{V_T}^{V_{DD}} C_g \text{cut} dV_{eq}
\]

\[
= \frac{1}{T} \left[ C_g \text{cut} V_T + C_g \text{cut} (V_{DD} - V_T) \right]
\]

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Substituting, we get
I = 100μA \quad V = 0.4V
Using C_{out} \text{ and } C_{gat} \text{ from previous example.}

\[ \frac{1}{100} \left( 3.15 + 15.165 \right) \Rightarrow 181.65ps \]

Problem 3. (5pt) Wire Delays
a) (3 pt) wire delay from node 0 to node 2, 4, i

node0-node2 delay:  \( C_1 R_1 + (R_1 + R_2)C_2 + C_3 R_1 + C_4 R_1 + C_i R_1 \)

node0-node4 delay:  \( C_1 R_1 + (R_1 + R_3)C_3 + (R_1 + R_2 + R_3)C_4 + R_i C_2 + C_i (R_1 + R_3) \)

node0-nodei delay:  \( C_1 R_1 + C_3 (R_1 + R_4) + C_i (R_1 + R_1 + R_3) + R_i (C_2 + C_4) \)
b) (2pt) if the gate delays are known as $T_g1$, $T_g2$, $T_g3$, $T_g4$, what is the delay from in1 to out2 and from in1 to out3?

\[
\tau_{in1-out2} = T_g1 + (\text{node0}-\text{node2}) + T_g2 \\
\text{Wire delay}
\]

\[
\tau_{in1-out3} = T_g1 + (\text{node0}-\text{node1}) + T_g3 \\
\text{Wire delay} \quad \text{gate delay}
\]

Wire delays computed in previous problem.