An Example of Scalable Design Rules for Integrated Circuit Layout

The following pages contain an example of a typical set of design rules that is used by the MOSIS integrated circuit fabrication service. The symbol names, colors, and patterns for the different layers refer to the MAGIC layout software package.

### MOSIS CMOS Scalable Rules

<table>
<thead>
<tr>
<th>LAYER</th>
<th>SYMBOL</th>
<th>MIN. DIM.</th>
<th>COLOR</th>
<th>PATTERN</th>
</tr>
</thead>
<tbody>
<tr>
<td>NDIFFUSION</td>
<td>ndiff</td>
<td>3</td>
<td>green</td>
<td></td>
</tr>
<tr>
<td>PDIFFUSION</td>
<td>pdiff</td>
<td>3</td>
<td>brown</td>
<td></td>
</tr>
<tr>
<td>POLYSILICON</td>
<td>poly</td>
<td>2</td>
<td>red</td>
<td></td>
</tr>
<tr>
<td>METAL1</td>
<td>m1</td>
<td>3</td>
<td>blue</td>
<td></td>
</tr>
<tr>
<td>METAL2</td>
<td>m2</td>
<td>3</td>
<td>purple</td>
<td></td>
</tr>
<tr>
<td>NWELL</td>
<td>nwell</td>
<td>10</td>
<td>lt. green</td>
<td></td>
</tr>
<tr>
<td>PWELL</td>
<td>pwell</td>
<td>10</td>
<td>lt. brown</td>
<td></td>
</tr>
<tr>
<td>CONTACT</td>
<td>m2c, pc, ndc, pdc, nnc, ppc</td>
<td>2</td>
<td>lt. brown</td>
<td>M1, M2</td>
</tr>
</tbody>
</table>

*ECE 474B/574B*

Digital Integrated Circuits
COMMENTS

1. ALL CONTACTS ARE WITH RESPECT TO THE METAL1 LAYER (e.g. pc= m1 to poly).

2. DIMENSIONS ARE IN UNITS OF LAMBDA FOR GENERAL LAYOUTS OR MICRONS FOR 2.0 MICRON TECHNOLOGY (LAMBDA = 1.0).

3. A SUBSTRATE OR WELL CONTACT MAY BE SHOWN BY A FREE STANDING CONTACT OR BY A DOUBLE CONTACT AT THE SOURCE OF A TRANSISTOR.

4. DIMENSIONS GIVEN ARE MINIMUM VALUES, EXCEPT FOR CONTACT SIZES WHICH MUST BE EXACTLY 2 X 2 AS SHOWN.

RULES

A. ACTIVE (TRANSISTOR)

SUMMARY OF RULES:
1. MINIMUM DIFFUSION WIDTH = 3
2. MINIMUM POLY WIDTH = 2
3. MINIMUM SPACING OF FIELD POLY TO DIFFUSION = 1
4. POLY GATE OVERLAP OF DIFFUSION = 2
5. EXTENSION OF DIFFUSION BEYOND POLY GATE = 3
6. MINIMUM POLY GATE TO CONTACT = 2
7. CONTACT IS EXACTLY 2 X 2
B. GENERAL WIDTHS AND SPACINGS

**SUMMARY OF RULES:**

1. MINIMUM POLY WIDTH = 2  
   MINIMUM POLY SPACING = 2
2. MINIMUM DIFFUSION WIDTH = 3  
   MINIMUM DIFFUSION SPACING = 3
3. MINIMUM METAL1 WIDTH = 3  
   MINIMUM METAL1 SPACING = 3
4. MINIMUM METAL2 WIDTH = 3  
   MINIMUM METAL2 SPACING = 4
5. MINIMUM WELL WIDTH = 10  
   MINIMUM WELL SPACING = 4  
   MIN PWELL TO NWELL SPACING = 9
6. DIFFUSION TO WELL EDGE = 5
7. WELL CONTACT TO WELL EDGE = 3
8. MIN ACTIVE TO WELL CONTACT = 3
9. EXTERNAL DIFFUSION TO WELL = 5
10. CONTACT WIDTH = 2
11. CONTACT OVERLAP = 1  
    (DIFF, M1, M2, POLY)
12. MIN OVERLAP PLUS CONTACT = 4
C. OTHER CONTACTS

SUMMARY OF RULES:
1. MULTIPLE POLY/DIFFUSION CONTACT SPACING = 2
2. POLY/DIFF/METAL OVERLAP OF CONTACT = 1
3. CONTACT TO TRANSISTOR CHANNEL = 2
4. DIFF CONTACT TO POLY CONTACT = 4
5. FIELD POLY TO DIFF W/ MULTIPLE CONTACTS = 2
6. POLY CONTACT TO POLY CONTACT = 5
7. POLY CONTACT TO FIELD POLY = 4
8. METAL2 ONLY CONNECTS TO METAL 1
9. A VIA MUST BE ON A FLAT SURFACE BY SPACING CONTACTS 3 UNITS WHEN NO DIFF/POLY IS UNDERNEATH OR EXTENDING DIFF/POLY 2 UNITS BEYOND THE VIA ON ALL SIDES. UNRELATED DIFF/POLY TO VIA = 2.
10. CONNECT METAL2 TO DIFF/POLY BY FORMING A METAL2 TO METAL1 VIA AND THEN A METAL1 TO DIFF OR POLY CONTACT.
D. EXAMPLE LAYOUT