Lect#25
Timing (cont)

1. True Single-phase Clocked Register (TSPCR)

CMOS skew-tolerant, but needs two phases.

Positive latches

Negative latches

Including logic into the latch

And latch.
2. Synchronous Design  
(refer to pp 495)

10.3

Global synchronous, local asynchronous

![Clock Synchronisation Diagram]

- \( t_{clk1}, t_{clk2} \)
- \( t_{cd}, t_{cq}, t_{c-q} \): minimum propagation delay, contamination delay
- \( t_{su}, t_{thoid} \)
- \( t_{logic}, t_{cd}, t_{logic} \)
- \( t_{aki}, t_{clk2} \)

Ideally, \( t_{clk1} = t_{clk2} \).

\[ T \geq t_{c-q} + t_{logic} + t_{su} \]

\[ t_{thoid} \leq t_{c-q}, t_{cd} + t_{logic}, t_{cd} \]

0 clock skew

\[ \text{clk1} \]

\[ \text{clk2} \]
\[ T + \delta \geq t_{c-g} + t_{\text{logic}} + t_{su}. \quad \delta \geq 0 \]

\[ \Rightarrow T \geq t_{c-g} + t_{\text{logic}} + t_{su} - \delta \]

*Improve the performance!!!*

However,

\[ \delta + t_{\text{hold}} \leq t_{c-g, cd} + t_{\text{logic, cd}}. \]

\[ C_{lki} \]

\[ C_{lk2} \]

\[ t_{su} \leq t_{\text{hold, } 1} \]

\[ I_n \]

\[ Q_1 \]

\[ t_{\text{hold}} \leq t_{c-g, cd} + t_{\text{logic, cd}} \leq t_{\text{delay, of } c-g, \text{logic}} \]
Clock jitter:

\[ t_{\text{CLK}} - 2t_{\text{jitter}} \geq t_{c-q} + t_{\text{logic}} + t_{su} \]

Combined Impact of skew and jitter:

\[ T_{\text{CLK}} + \delta - 2t_{\text{jitter}} \geq t_{c-q} + t_{\text{logic}} + t_{su} \]
\[ S + \text{thiold} + 2 \cdot \text{jitter} < t_{ca} - \sigma, \text{cd} + t_{\text{capacity, cd}} \]

10.1, 10.2, 10.3 (not 10.3.4)

Memory:

P640
Example 12.3
Example 12.4
12.7

Section 12.23