Timing Metrics for sequential

1. Three important timing parameters associated with a register:
   - \( t_{su} \): setup time - \( D \) must be valid before clock transition (or clock edge)
   - \( t_{hold} \): hold time - \( D \) must remain valid after clock transition
   - \( t_{prop} \): propagation delay - \( D \) is copied to \( Q \) after a worst case propagation delay after clk transition

\[\text{CLK} \]
\[\text{D} \]
\[\text{Q} \]

\( t_{su}, t_{hold} \) decide duration of DATA
\( t_{prop} \) is prop delay
In timing graph.

\[ D = Q^a \]

\[ \text{CLK} \]

\[ A \rightarrow F \]
\[ B \rightarrow F \]
\[ t_{af} \]
\[ t_{bf} \]

**Combination logic**

\[ R \rightarrow Q_1 \]
\[ D \]
\[ \text{CLK} \]
\[ Q_1 \]
\[ \text{DATA} \]
\[ t_{c-eq} + t_{plogic} + t_{su} \]

\[ T \geq t_{c-eq} + t_{plogic} + t_{su} \]

\[ t_{cd\text{register}} + t_{cd\text{logic}} \geq t_{hold} \]

You don't need high \( t_{hold} \)

\( cd \): contamination delay or minimum delay
thold is more likely to be the problem (depends on internal circuit design)

2. Static latches and Registers (review)

We first analyze the behavior and then find out the timing info.
"0 to 1" negative edge triggered

CIRCUIT SCHEMATIC
\[ \overline{CK} = 1 \quad (\text{clk is low}) \]

- \( T_1 \) on \quad \overline{QM} = D \\
- \( T_2 \) off \\
- \( \overline{QM} = D \) \\
- \( T_3 \) off \quad Q \text{ No Change} \\
- \( T_4 \) off \quad \begin{align*}
& I_1 \to I_6 \\
& \text{hold the Q state}
\end{align*}

\[ CK = 1, \]

- \( T_1 \) off \quad I_2 \quad I_3 \quad \text{hold QM} \\
- \( T_2 \) on \\
- \( T_4 \) off \\
- \( T_3 \) on \quad Q = QM

\[ \text{tsu, thold t c-\delta:} \]

Assume \( \text{tpd-inv, tpd-tx} \)

\[ \text{tcd} = 0 \quad \overline{CK} \quad \text{clk same time arrival} \]

\[ \text{tsu: KEEP IN MIND: only compare to rising edge} \]

\[ \begin{align*}
\text{t}_{\text{su}} &= 3 \text{t}_{\text{pd-inv}} + \text{t}_{\text{pd-tx}} \\
\text{t}_{\text{d}} &= \text{t}_{\text{pd-tx}} + \text{t}_{\text{pd-in}} \\
\overline{\text{thold}} &= ? \\
\text{tcd} &= 0 \quad \text{(our assumption)} \\
\text{thold} &= 0 \quad \text{because T1 is off after } \overline{CK} = 1.
\end{align*} \]
3. Dynamic latches and Registers need periodic refresh.

**DTGETR**

Dynamic Transmission-Gate Edge-Triggered Register

When $\overline{\text{CLK}} = 0$, $D \rightarrow T_1 \rightarrow Z_1 \rightarrow T_2$

At $C_1$, $I_1 \rightarrow T_2$

$C_1 + T_1$'s junction caps + gate cap of $I_1$

In hw:

This is part from dynamic register.

The slave stage is in hold mode (high impedance)

When $\overline{\text{CLK}} = 1$

$T_2$ on $T_1$ off.

$t_{su}$, $t_{su} = t_{T_1} + t_{Z_2}$

$t_{hold} = 0$ ($T_2$ off if $\overline{\text{CLK}} = 1$)

$t_{c-Q} = t_{T_2} + t_{Z_3}$
3. \( C^2\text{MOS} - \) A Clock-Skew Insensitive Approach

What is clock-skew?

When \( \text{clk} \) at 1 and 2 may be different.

\[ \text{clk} \]

\[ \text{clk} \]

\[ \text{clk} \]

\[ \text{clk} \]

\[ \text{clk} \]

\[ \text{clk} \]

\[ \text{clk} \]

\[ \text{clk} \]

\[ \text{clk} \]

1. \( \text{clk} = 0 \)
   \( M_3 \) on  \( M_4 \) on
   \( M_2, M_1 \) depend on \( D \)

2. \( \text{clk} = 1 \)
   \( M_3 \) off  \( M_5 \) on
   \( M_4 \) off  \( M_7 \) on

Because \( \overline{\text{clk}}, \text{clk} \) on same master or slave, no concern about \( \text{clk}, \overline{\text{clk}} \) skew.
\[ t_{overlap} \leq t_{T_1} + t_{I_1} + t_{T_2} \]

\[ t_{threshold} > t_{overlap} \]

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For CMOS:

- \( \overline{CLK} \rightarrow 0 \quad (0,0) \) overlap. \( M_4 \) off
- \( \overline{CLK} \rightarrow 1 \quad M_3 \) on
- No change on \( x \)
- No change on \( Q \)