Lec#20. Ratioed logic
and transmission gate.

Today we talk about
1. Ratioed logic

2. transmission gate

3. HW#3. (if we have time)

1. Ratioed logic:

a. Why? Attempt to reduce the number of transistors required to implement a given function. Tradeoff: reduced robustness, extra power dissipation

b. How? 

\[
\begin{align*}
\text{PDN} & \quad \text{PDN} \\
\text{GND} & \quad \text{GND} \\
\text{VDD} & \quad \text{VDD} \\
\text{out} & \quad \text{out}
\end{align*}
\]

\[2N \text{ transistors} \Rightarrow \frac{N+1}{N+1} \text{ transistors.}\]

Let us take a close look at...
We have static power consumption and reduced noise margin!!

Let us compute the dc-transfer VTC for pseudo-NMOS (only one pmos, everything is NMOS).

\[ V_{OL} \approx \frac{W_p}{N} \times V_{SAT} \]

NMOS in linear mode
PMOS in saturated (a saturated)

\[ V_{OL} \approx \frac{W_p}{W_n} \times V_{SAT} \]

\[ \frac{W}{L_p} = 4 \rightarrow V_{OL} = 0.66 \, V \]
\[ \frac{W}{L_p} = 0.25 \rightarrow V_{OL} = 0.03 \, V \]

Good!

but you have static power consumption!!
Differential Cascode Voltage Switch Logic (DCVSL)

PDN1 Conducts  PDN2 off
PDN1 off  PDN2 Conducts

When PDN1 conducts,
- OUT low,
- NOT high impedance.

Since M2 off, PDN2 off
(-float),
possible to discharge OUT
all the way to GND.

Because: when M2 off, OUT discharge
to VDD - (Vth), it turns on
M2, M1 charges OUT, turns
off M1, M3 off, let "OUT"
to discharge to "GND".
design a gate with DCVSL

\[ f = \overline{AB} \]

\[ \overline{\text{out}} = \overline{AB} \]

\[ \overline{M_1} \quad \overline{M_2} \quad \overline{M_3} \quad M_4 \]

\[ \overline{V_{out}} \quad \overline{V_{out}} \]

\[ V_{in} \quad V_{out} \]

\[ V_{in} \quad V_{out} \]
2. Transmission gate (or pass-transistor logic)

\[ F = A \bar{B} \]

- If \( B = 1 \), \( M_1 \) on.
- If \( B = 0 \), \( M_2 \) on, \( M_1 \) off.

We know already that nmos "good" to pass '0' but "bad" to "pass '1'.

\[ V_{DD} - V_{Th} \]

\[ V_x = V_{DD} - (V_{Th} + \gamma(\sqrt{2V_x + V_s} - \sqrt{2V_x}) \]

trick: Don't connect pass-transistor together.

\[ V_y = V_{DD} - V_{Th} - V_{Th} \]

bad choice

OK choice!
How to build Robust and Efficient Pass-transistor gates?

Strategy 1: Level Restoration (Footer or header)

- How to size $M_r$:
  1. First fix size of $M_1$, $M_2$, $M_3$.
     Use hyspice to modulate $M_r$.
  2. $M_r$ size always small.

Strategy 2: Transmission Gate logic

- If $C = 1$, $B = A$. Strong pass for both "0" and "1".
- If $C = 0$, cutoff.

$\frac{R_p}{R_n}$ during $L \rightarrow H$ for output goes through different modes.

If $V_b$ is low $V_{MOS}$ sat, linear, eff. PMOS sat.

$R_p = \frac{V_{out} - V_{dd}}{I_{op}} = \frac{V_{out} - V_{dd}}{K_p \left( (-V_{dd} - V_{TP}) \left( V_{out} - V_{dd} \right) - \frac{(V_{out} - V_{dd})^2}{2} \right)}$

\[= \frac{1}{K_p (-V_{dd} - V_{TP})} \]
$R_n$ changes.

![Graph showing $R_p$, $R_n$, and $R_n/|R_p|$ relationships.]

$E_{more}$