Lec#18 Design Complex SCCD gate

1. SCCD is input pattern dependent

- **Example**
  - When $A=0$ and $B=0$, charging $C_L$
  - When $A=1$ and $B=1$, discharging $C_L$

- **Pun strong**
  - $\frac{(W/L)_p}{(W/L)_N}$
  - Current ratio, $V_{in}$ makes difference

- **Conditions**
  - $A=1$, $B=0$ → $1$
  - $A=0$, $B=1$ → $1$

- **Node $i$**

- $V_{GSm_1} = V_A - V_{os n_1}$
- $V_{GSm_2} = V_B$

- $V_{Th n_1} = V_{Tho} + \frac{V_i}{\sqrt{\frac{2(2p_n+1)}{12N}}} - \sqrt{\frac{2p_n}{12N}}$
  - $V_i$ makes difference

- $V_{Th n_2} = V_{Tho}$

- So $V_{Th n_1} > V_{Th n_2}$
A = 1 \quad M_P^1 \text{ is off}
V_{at} \text{ for } M_{N_1} \text{ is always } V_{DD}

B = 1 \quad M_P^2 \text{ is off}

For propagation delay of Complementary CMOS gates, we can use first order switch model.

You can in fact use Elmore delay model.
Example:

\[ C_1 : C_{d1} + C_{d2} + 2C_{gd1} + 2C_{gs2} \]
\[ C_2 : C_{d2} + C_{d3} + 2C_{gd2} + 2C_{gs3} \]
\[ C_3 : C_{d3} + C_{d4} + 2C_{gd3} + 2C_{gs4} \]
\[ C_L : C_{d4} + 2C_{gd4} + C_{d5} + C_{d6} + C_{d7} + C_{d8} + 2C_{gd5} + 2C_{gd6} + 2C_{gd7} + 2C_{gd8} \]

**How to size complex SCCD gates?**

Sizing is only effective if the load is dominate by fan out.
Inverter:

\[ t_p = t_{po} \left( 1 + \frac{C_{ext}}{\gamma C_0} \right) = t_{po} (1 + \frac{f}{\gamma}) \]

extension to general complex gates.

\[ t_p = t_{po} (p + g_f/\gamma) \]

- \( p \): ratio of intrinsic delay of complex gate and simple inverter.
- \( f \): effective fan out.
- \( g \): logic effort.
- \( \gamma = \frac{C_{ext}}{C_0} \)
logical effort: for a given load, complex gates have to work harder than an inverter to produce a similar response, or how much more input capacitance a gate represents to deliver the same output current as an inverter?

\[ C_{g_{\text{p}}} = \frac{C_{\text{ox}} W L}{2} + 2 C_{\text{inv}} \]
\[ C_{g_{\text{p}} p} = \frac{2}{3} C_{\text{ox}} W L + 2 C_{\text{inv}} \]

minimum-sized symmetrical inverter.

So \( C_{g_{\text{p}}} = 2 C_{g_{n}} \)
\( C_{g_{\text{inv}}} = C_{\text{unit}} \)

\( C_{g_{\text{total}}} = 3 C_{g_{n}} \)
\( C_{g} = 3 C_{\text{unit}} \)

\[ g = \frac{C_{g_{\text{complex.gate}}}}{C_{g_{\text{inv}}}} \]

\[ g_{\text{complex.gate}} = 4 C_{\text{unit}} \]

So \( g = \frac{4}{3} \)

\[ g = ? \quad g = \frac{5}{3} \]
Extension to path, branch

\[ R \propto \frac{1}{(z)} \]

\[ R \text{ if } \text{w} \quad \text{or } R \text{ if } \text{w} \]

So, series connection case \( \rightarrow \) sizing factor.

Parallel connection case

path:

\[ t_p = \sum_{j=1}^{N} t_{p_j} = t_{p0} \sum_{j=1}^{N} \left( p_j + \frac{f_j a_j}{2} \right) \]

\[ G = \sum_{i=1}^{N} g_i \quad F = \frac{C_L}{C_g} \]

\[ b = \frac{\text{Con-path} + \text{Off-path}}{\text{Con-path}} \]

\[ B = \frac{N}{i} b \]

\[ H = GFb \]