

David Schwartz

dmschwar@email.arizona.edu

<http://www.ece.arizona.edu/~dmschwar>

- EDUCATION** **University of Arizona**, Tucson, AZ **Aug. 2017 - Present;**
Ph.D. in Electrical and Computer Engineering
University of Arizona, Tucson, AZ **Aug. 2015 - May 2017; GPA: 3.625/4.0**
M.S. in Electrical and Computer Engineering
University of Arizona, Tucson, AZ **Aug. 2010 - May 2015; GPA: 3.164/4.0**
B.S. in Electrical and Computer Engineering
B.S. in Mathematics
- EXPERIENCE** **Graduate Teaching Assistant, Univ. of Arizona (Aug. 2017 - Present)**
Assisted by grading and holding office hours for ECE 275: Computer Programming for Engineering Applications II (Supervisor: Garrett Vanhoy)
Mathematics Tutor, Univ. of Arizona, (Aug 2017 - Present)
Tutored students with learning challenges in undergraduate mathematics and science courses (Supervisor: Geoff Thames)
Graduate Research Assistant, Univ. of Arizona (Aug. 2015 - May 2017)
Research on information theory, coding theory, detection and estimation, investigated coding and information theoretic properties of neural codes utilized in spatial navigation tasks (Supervisor: Dr. O. Ozan Koyluoglu)
Graduate Teaching Assistant, Univ. of Arizona (Aug. 2015 - May 2016)
Assisted Dr. Ali Bilgin and Dr. Siyang Cao in teaching, writing assignments, and grading for the Matlab component of ECE 310: Applications of Engineering Mathematics
Computer Engineering Intern, Univ. of Arizona (Jul. 2014 - Aug. 2015)
Developed 10GbE transceivers to safely transport measurements acquired by muon detectors at the large hadron collider and verified that designs consistently met specified power and latency constraints (Supervisor: Dr. Ken Johns)
Undergraduate Research Assistant, Univ. of Arizona, (Jan. 2012 - Jan. 2014)
Implemented and tested an ultra low power (on the order of μ Watts) activity driven forest fire monitor in FPGA fabric with a globally asynchronous, locally synchronous, multi-clock architecture (Supervisor: Dr. Roman Lysecky)
- RELEVANT COURSEWORK** **M.S.:** Information Theory, Random Processes, Detection and Estimation Theory, Digital Signal Processing, Channel Coding, Quantitative Modeling of Biological Systems, Machine Learning, Topics in Network Information Theory
B.S.: Design of Complex Computer Systems, Principles of AI, Automatic Control, Complexity Theory, Computational Techniques, Microprocessor Organization, Object Oriented Software Design, Fundamentals of Computer Architecture, Signals and Systems, Electronic Circuits, Circuit Theory, Topological Spaces, Real Analysis of One Variable, Real Analysis of Several Variables, Complex Variables, Advanced Applied Analysis, First Course in Abstract Algebra, Second Course in Abstract Algebra
- HONORS and AWARDS** Graduate Tuition Scholarship at The University of Arizona
Won ‘Most Robust Design’ award for Senior Design Project at The University of Arizona
- PUBLICATIONS** · D. Schwartz, O. O. Koyluoglu, “On the organization of grid and place cells: Neural de-noising via subspace learning” Submitted for publication, *Neural Computation*. [Online]. Available: arXiv:1712.04602
· D. Schwartz, O. O. Koyluoglu, “Neural noise improves path representation in a simulated network of grid, place, and time cells” *Cosyne Abstracts 2017*, Salt Lake City, USA
· M.J. Ragone, S. Gianelli, D. Schwartz, L. Su, O.O. Koyluoglu, J.-M. Fellous, “The role of hippocampal replay in a computational model of path learning” Program No. 263.14. 2016 Neuroscience Meeting Planner. San Diego, CA: Society for Neuroscience, 2016. Online
· D. Schwartz, O.O. Koyluoglu, “A hybrid code from grid and place cells” Program No. 183.26. 2016 Neuroscience Meeting Planner. San Diego, CA: Society for Neuroscience, 2016. Online
· T. Pifer, D. Schwartz, R. Lysecky, C. Seo, and B. P. Zeigler, “Discrete event system specification, synthesis, and optimization of low-power FPGA-based embedded systems” 2013 International Conference on Field-Programmable Technology (FPT)
- SKILLS** **Programming Languages:** C, C++, Java, Matlab, Python, Ruby, VHDL, Verilog
Other Computer Tools: Latex, Unix, Xilinx ISE, XPS, Vivado, Synplify
- OUTREACH and SERVICE** Judged at SARSEF science fair in Tucson in 2016 and 2017
Reviewed a paper for publication at IEEE ICC’17 (International Conference on Communications 2017)