ANALYSIS OF SWITCHING TRANSIENTS IN A DYNAMICALLY RECONFIGURABLE ANALOG/DIGITAL HARDWARE

Cornel Reiser[1], Lech Znamirowski[2], Olgierd A. Palusinski[3], Sarma B. K. Vrudhula[3]

[1] Institut für Theoretische Elektrotechnik und Messtechnik, University of Karlsruhe, 76128 Karlsruhe, Germany
E-mail: cornel.reiser@stud.uni-karlsruhe.de
[3] Instytut Informatyki, Technical University of Silesia, Ul. Akademicka16, 44-100 Gliwice, Poland
E-mail: lznamiro@top.iinf.polsl.gliwice.pl
[3] Department of Electrical and Computer Engineering, University of Arizona, Tucson, AZ 85721, USA
E-mail: palusinski@ece.arizona.edu

KEYWORDS

Reconfigurable Hardware, Mixed-signal Circuits, Adaptive Filtering, Field Programmable Analog Arrays (FPAA), Field Programmable Gate Arrays (FPGA)

ABSTRACT

This paper presents an investigation of dynamically reconfigurable mixed-signal circuit constructed using a digital control system and the new technology of Field Programmable Analog Arrays (FPAA). A Motorola FPAA described in this paper can be used to build filters for analog signals as well as other kinds of analog applications implemented in switched capacitor technology (S/C-technology). The experimental studies described, take advantage of performance and programmability of the FPAA for filtering of an analog signal. The circuit structure is based on 2 parallel FPAA chips, analog multiplexer and multiplexer's control logic controlled by a digital system such as a PC or a Field Programmable Gate Array (FPGA). Dynamic reconfiguration is used in this system for adaptive filtering, or adaptive processing in general. Modeling and measurements of the transition behavior of the switching process between the 2 FPAA chips and analysis of limitations imposed by hardware imperfections will be presented. The experimental system assembled in this work is an excellent vehicle to learn about intricacies in performance of mixed-signal circuits and is used for verification of theoretical predictions and model validation/modification.

1. INTRODUCTION

Digital circuits can be used to implement high-accuracy and high-complexity signal processing algorithms, typically for low frequency signals where power dissipation during the operations is not critical. Analog circuits offer advantages in applications where signal frequencies are high and low power dissipation is essential. However, the accuracy of analog circuits is limited and they can not be used to implement algorithms of high complexity. As the complexity of modern

processing systems grows, the traditional design with strict separation of analog and digital functions becomes impractical. Often times, it is desirable to have flexible and programmable systems such that partitioning into analog and digital circuitry can be changed during processing. Processing in a large system is assigned to analog and digital circuits to take advantage of specific circuit properties for overall performance optimization, such as power minimization. If the processing requirements and algorithms change over time, the optimal assignment of processing functions may change and dynamic reassignment of functions and reconfiguration of circuits may be necessary. A typical technology of analog circuits did not provide so far the capability of changing the circuitry once it was built up. The new technology of Field Programmable Analog Arrays (FPAA) in combination with the well known technology of Field Programmable Gate Arrays (FPGA) provides a basis for the development of a dynamically reconfigurable analog/digital hardware. Using two or even more of these devices in parallel it is possible to reprogram the system and reassign the circuits in real time. Switching the outputs of the FPAAs provides an uninterrupted processing of the input signal. To optimize the transitions of the switching and to fasten the reconfiguration process it is necessary to analyze the dynamic time behavior of the reconfiguration and to model the transitions between the diverse chip in an experimental setup. Such a mixed-signal circuit is very suitable for applications in mobile systems, such as cell phones and other portable telecommunication systems in general, because power dissipation can be reduced by proper assignment of hardware processing functions to analog and digital circuits. Dynamically reprogrammable circuits can also adapt to changing external conditions such as background noises in a portable equipment, which may vary with the location.

2. THE FIELD PROGRAMMABLE ANALOG ARRAY (FPAA)

A Field Programmable Analog Array (FPAA), built in CMOS technology, contains uncommitted operational amplifiers, switches, and banks of programmable switched capacitors (S/C) and can be used to build filters for analog signals as well as a large number of diverse analog applications. The parameters of a given application, such as a filter, are functions of the capacitor values. The chip is divided into 20 identical, configurable analog blocks (CABs), each composed of an operational amplifier, five capacitor banks, and switches that can be used to interconnect the cell components and determine their operation. There are both static and dynamic CMOS switches. The static switches are used to determine the configuration of cell components and inter-cell connections. These switch settings are determined once during the programming phase of an application after which they remain unchanged. The dynamic switches are associated with capacitors and are switched periodically during the circuit operation changing the effective function of capacitors as typically exploited in switched capacitor (S/C) circuits. Both static and dynamic switches are electronically controlled and thus the functionality of each CAB, the capacitor sizes, and the interconnections between CABs are programmable. As a result many diverse circuit architectures can be implemented.

The FPAA used in this study is Motorola's MPAA020 which contains 41 operational amplifiers, 100 programmable capacitors, 6864 electronic switches arranged into the 20 CABs, and 13 input/output buffers. The array is structured in a grid that contains the 20 CABs arranged in a 4x5 matrix. Configuring an analog design within the array is performed by downloading 6K bits of data via RS232 communications from a PC or EPROM. The data stream contains information to configure the individual cells, the cell to cell interconnections, internal voltage reference as well as the input and output connections. During the configuration download process all cells are placed in a power-down mode to protect the CABs against undesirable high currents. The switches allow control over the circuit connectivity and capacitor values in addition to other features.

The complexity of control is so high that a supporting software was developed to facilitate the chip programming. The software allows a user to easily manipulate these field-programmable switches in order to implement a specific circuit. The chip programming software is called EasyAnalog™ and runs under Windows 3.1, Windows 95, and Windows NT operating systems. The basic interface window of EasyAnalog™ displays a simplified view of 20 CABs, 13 I/O isolation amplifiers, and inter-cell connecting lines. With a "point and click" action the user can select and place "macros" from a function library onto the chip in any feasible cell location.

Each macro is a pre-configured sub-circuit such as a gain-stage, filter, full-wave rectifier, or biquad, just to mention some examples. Several macros can be placed onto the chip and "wired" together as required by an application. There are also some "pre-wired" application circuits, stored in a library, which can be selected and placed on the chip. Parameters of the library components can be selected and changed, as needed in the application, using pull-down menus and pop-up windows. (Birk 1998; Palusinski *et al*. 1998)

The FPAA technology is suitable for numerous engineering applications like electrical signal filtering, construction of controllers and phase correctors for continuous and sampled data feedback systems, conditioning of sensor signals and signal generation. The power of the FPAA is that it can be reconfigured "on the fly" to implement different device or parameter settings (Znamirowski, Palusinski 1998) and that's why the chip is so suitable for dynamic reconfiguration as it is demonstrated in the experimental investigations presented in this paper.

3. SYSTEM DESCRIPTION

The basic concept of a dynamically reconfigurable mixed-signal hardware is presented here using an example of system composed of 2 parallel FPAAs, analog multiplexer and multiplexer's control logic (addressing FPAA and switching time delay settings). In the reported experiments all the control was determined using a PC and the software EasyAnalog™.

The experimental setup was primarily intended for investigations of switching inaccuracies and performance imperfections caused by the hardware. A more sophisticated control system, implemented on FPGA will be used to analyze the input signal and generate the desired filter function. FPGA will provide a time delay for the switching in order to minimize the effect of perturbations that are investigated in this work.

The block diagram of the system is shown in Figure 1.

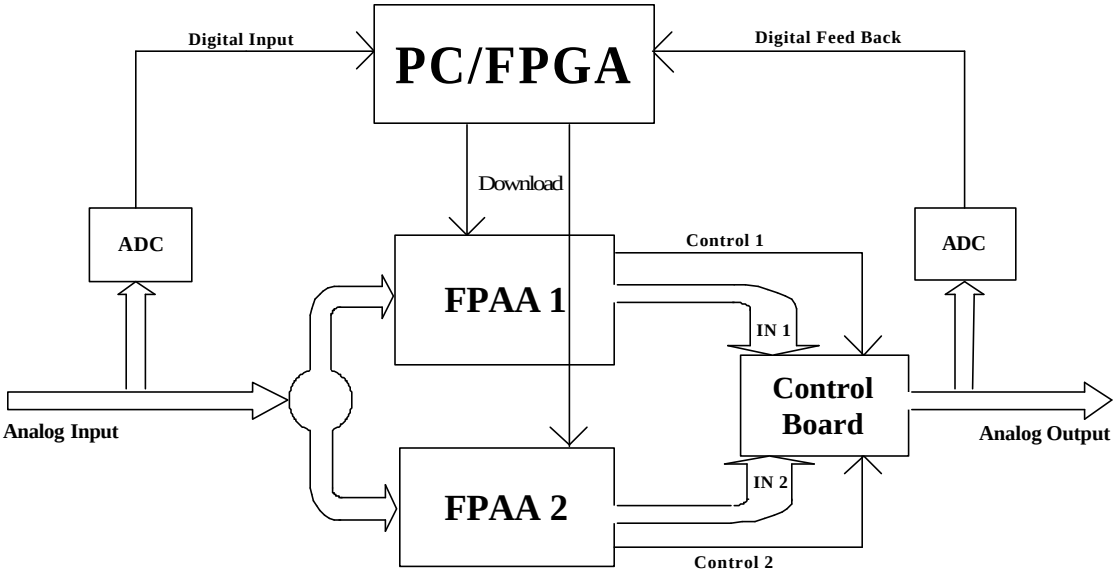

Figure 1. Block diagram of the system composed of 2 parallel FPAAs.

A control signal for the multiplexer is generated on the FPAA output. When the FPAA starts to work after reconfiguration, a 'HIGH'-signal appears at an output pin that enters into an adjustable time delay circuit on the control board and then to the multiplexer to interchange the analog outputs of the FPAAs. The time delay circuit is established in order to introduce a time lag between the end of the reconfiguration phase, when the reprogrammed FPAA starts processing the input signal, and the physical switching of the multiplexer to the output of the reconfigured FPAA. In this system one FPAA can filter the analog input signal while the second one is 'off-line' waiting for reprogramming. After reconfiguration the multiplexer switches from the first to the reconfigured FPAA and then the other one is ready for reprogramming. The system using 2 FPAAs provides a steady output signal without an interruption when redefinition of the analog filter function is needed, such as changing the quality factor or adjusting the corner frequency. The described process is illustrated in the timing diagram in Figure 2.

A complicating factor of the dynamic reconfiguration is the transition behavior of the switching from one FPAA to the other. After the FPAA is reprogrammed it cannot be put immediately "on-line" because the signal needs some time to settle and reach a steady state. That's why it is necessary to provide a time delay between the end of the programming phase and the actual physical switching. During programming of a FPAA the chip is reset and all capacitors are discharged. The output is also set to earth ground in contrast to the signal ground of 2.5V established on the chip during processing. Considering the 'jump' of 2.5V from earth to signal ground the transition behavior can be modeled as a step response of a system of second order with typical exponential settling behavior of a FPAA biquad.

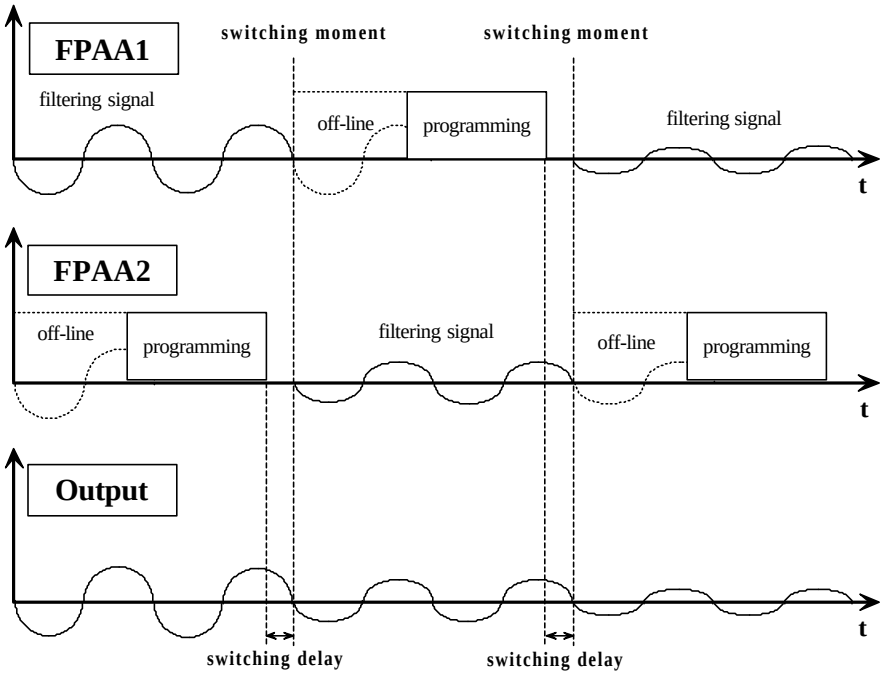

Figure 2. Timing diagram of reprogramming and filtering of 2 parallel FPAAs for uninterrupted processing of an analog input signal.

The circuit will be analyzed using sinusoidal analog input signals with small amplitudes as typically used in data processing applications. A typical example of a measurement performed using a sinusoidal input signal is given in Figure 3.

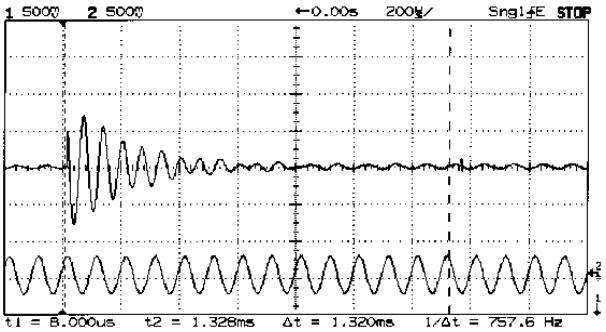

Figure 3. Settling behavior of band pass filter after switching.

During various measurements it was observed that for both inputs, step function and sinusoidal signal, the output is forced into the same exponential envelope. This means that the measured settling time of a step input is also the time period within which the sinusoidal signal settles in. Thus, a constant step function as the input signal was utilized during the measurements of the settling time.

Another important aspect of the switching process is the moment of switching between two settled FPAAs within the period of the sinusoidal signal. For example, if the user changes the quality factor of a low-pass filter and switches near the peak of the sinusoidal input signal, there will be a jump in the output as illustrated in the Figure 4a. Such a jump causes an injection of high frequency components that should be avoided in filtering applications, particularly using a low-pass filter. Therefore, in the case of changing the quality factor Q of the filter, it is necessary to switch at the zero crossing of the sinusoidal signal to minimize undesirable jumps of the amplitude as shown in the right graph of Figure 4.

However, if the corner frequency of the filter or the whole filter in general will be changed, the user has to deal with discontinuities in the amplitude as well as a phase shift and the determination of the switching moment is more involved.

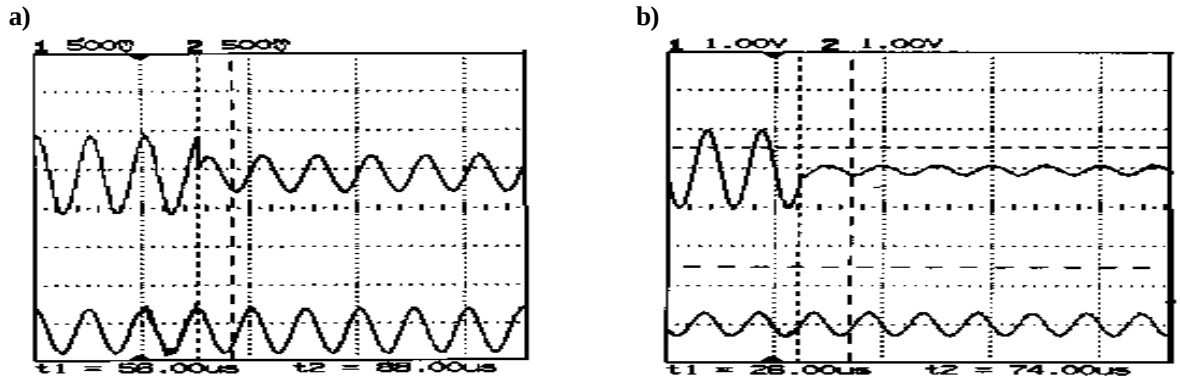

Figure 4. Switching at zero-crossing after time delay; a) switching near the peak, b) switching close to the zero-crossing.

When the control system is implemented on a FPGA and a digital forward and backward loop is established, the input signal will be analyzed with regard to zero detection in order to switch exactly at the zero-crossing right after the time delay when the signal is settled in.

4. TIME RESPONSE OF SYSTEMS OF 2ND ORDER

The modeling for the settling time presented here is applicable to any second-order system (biquad). The transfer function of a low pass biquad is

$$H_{low\,pass}(s) = -\frac{4p^2 f_0^{\,2} G}{s^2 + \frac{2pf_0}{Q}s + 4p^2 f_0^{\,2}} \tag{1}$$

where G is the pass-band gain (DC-Gain), Q is the quality factor, and f_0 is the corner frequency of the filter. The time response of this system is characterized by the roots of the denominator polynomial $q(s)$, which in fact are the poles of the transfer function. The denominator polynomial $q(s)$ is therefore called the *characteristic polynomial* and

$$q(s) = 0 \tag{2}$$

is called the *characteristic equation*. The characteristic equation of the system under consideration is

$$s^2 + \frac{2\pi f_0}{Q} s + 4\pi^2 f_0^2 = 0 \tag{3}$$

For the unit-step input the Laplace inversion of the proper transfer function yields the output time response given by (Nagrath 1975)

$$h(t) = G\left\{1 - \frac{e^{-\frac{2\pi f_0}{2Q}t}}{\sqrt{(1-1/4Q^2)}} * \sin\left[2\pi f_0\sqrt{(1-1/4Q^2)}\,t + \tan^{-1}\sqrt{(4Q^2-1)}\right]\right\} \tag{4}$$

The steady-state $h(t)$ is given in a form

$$h_{ss} = \lim_{n\to\infty} h(t) = G \tag{5}$$

It can be observed that the time response $h(t)$ oscillates between a pair of envelopes before reaching steady-state for Q>0.5. The transient is comprised of a product of an exponentially decaying term $e^{-\frac{2\pi f_0}{2Q}t}$ and a sinusoidally oscillating term $\sin\left[2\pi f_0\sqrt{(1-1/4Q^2)}\,t + \tan^{-1}\sqrt{(4Q^2-1)}\right]$.

The time constant of the exponential envelope is $T = \frac{Q}{\pi f_0}$. The settling time t_s is defined as the time period the signal needs to get within a certain tolerance band around the steady-state value and stays within these bounds. Considering only the exponentially decaying envelope for a tolerance band of 1% the settling time is given by

$$\frac{e^{-\frac{\pi f_0}{Q}t_s}}{\sqrt{(1-1/4Q^2)}} = 0.01 \tag{6}$$

For Q>>0.5 we have $e^{-\frac{\pi f_0}{Q}t_s} \approx 0.01$.

This yields the settling time t_s

$$t_s = \frac{4.605Q}{\pi f_0} \tag{7}$$

The equation (7) is applicable for all biquad filters.

5. MEASUREMENTS OF SETTLING TIME

The measurements were performed to verify the modeling of the settling time and to demonstrate that the described settling time model is applicable for both, an input step function and sinusoidal signals. A constant pass-band gain of G=1 was used in all measurements. The low resolution of the oscilloscope made it difficult to get the exact time when the signal deviation is smaller than 1%. Especially for low settling time values in the high frequency range and for quality factors

smaller than the value of one it is very difficult to obtain meaningful results, therefore there are only results of measurements with high Q ($1<Q<20$) filters presented. Additionally, the measured points were not situated exactly on a 'straight line'. In order to get a more meaningful analysis of the measured values, the measurements were approximated using a straight line determined by the method of linear regression (Weisberg 1985).

Cumulative results of measurements of the settling time as a function of the biquad quality factor are shown in Figure 5. The plot shows that indeed the behavior of a band pass biquad filter (high Q) with corner frequency of 50 kHz follows the analysis presented here.

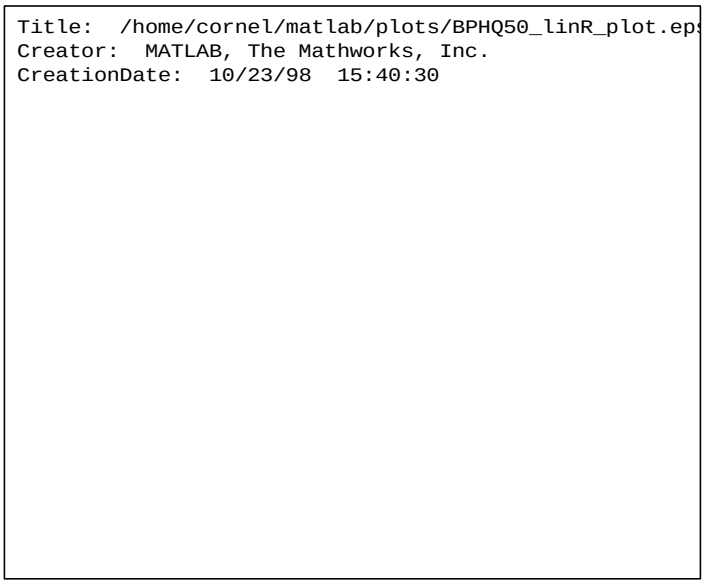

Figure 5. Settling behavior of band pass filter at corner frequency of 50 kHz.

The relative error between the calculated and the linear fit of this measured values is 1.48% and is mainly caused by reading errors of the oscilloscope due to the low resolution. The errors of other filter measurements are shown in Table-1.

Table-1. Relative errors of the measured settling time of various filters.

Filter	band pass	high pass	high pass	band stop	low pass
Corner frequency	10 kHz	25 kHz	100 kHz	50 kHz	25 kHz
Relative error	3.24%	2.05%	0.55%	1.33%	4.51%

The model of the settling behavior of biquad filters for various quality factors and corner frequencies is shown graphically in Figure 6.

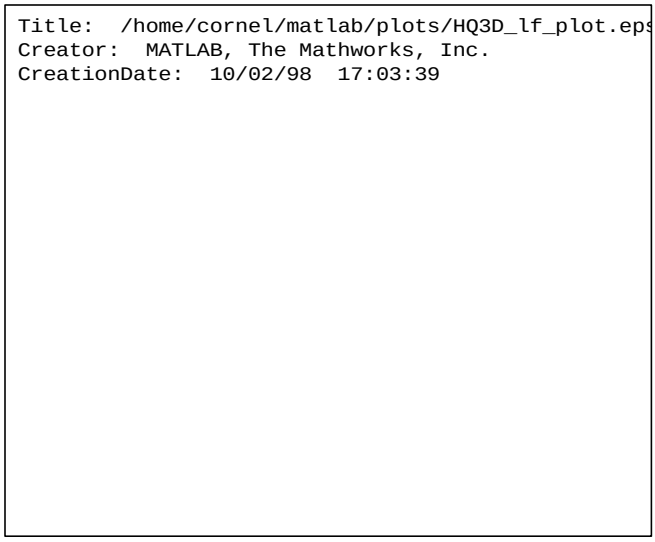

Figure 6. Settling time behavior versus quality factor and corner frequency.

This graph indicates that the settling time increases significantly with increasing quality factor, especially for very low corner frequencies. Therefore, the time delay for the switching of the output of the reconfigured FPAA has to be adjusted appropriately in order to avoid perturbations. This time delay must be indeed particularly long for the filters implemented with a low corner frequency and a high quality factor.

During various measurements it was discovered that for very low quality factors and high corner frequencies, which would allow for a very short settling time, the measured settling time was much higher than expected. Figure 7 shows this effect, where measurements with a high-Q high pass filter and the appropriate low-Q implementation were carried out for varying quality factors down to a minimum possible quality factor of Q=0.5.

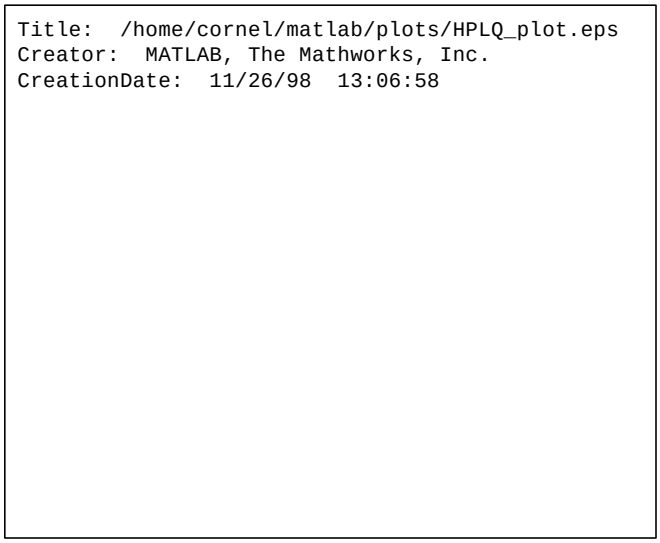

Figure 7. Measurements and the linear fit (for clarity, no high Q data presented) of a high pass filter in the low-Q range.

For the values smaller than Q=1 the measured settling time of the low-Q values is much higher than the linearized straight line fitted to the high-Q filter measurements. This effect, which can be observed on all filter measurements, is due to two reasons. First, a value for the settling time smaller than the minimum value of approximately $t_{s,min}$=50μs was never reached during any of the measurements (the technology of the FPAA seems to provide a kind of a 'natural boundary' for the speed that a signal needs to settle when the chip starts to work). Second, the reading errors are much bigger in the range of very low settling times because it is much more difficult to determine the settling time for a signal that reaches its steady-state in a very short time with low oscillations.

6. CASCADING BIQUADS

In practice, filters of higher order are commonly used because their better performance, such as for example the transition band, can be improved by a system of higher order. A filter of higher order is obtained cascading blocks of filters of first or second order. With the 20 analog cells of the FPAA it is possible to realize a filter of 20th order on one FPAA.

It is also necessary to investigate the settling behavior of these filters to develop a model for the prediction of the time delay that is needed for the reconfiguration process. In a simple experiment we measured the settling time of a series of increasing order of filters, generated by cascading identical high pass biquads. Thus, we measured first a filter of second order, then a filter of 4th order, built by two biquads, afterwards a 6th-order filter by three identical biquads, and so on up to a filter of 20th order, built by ten cascaded biquads. For each of these filters the settling time was measured with varying corner frequencies. A quality factor of Q=0.707 was used. Figure 8 shows the measured data, the curve with the biggest settling time values correspondents to the system of 20th order and that with the smallest value to the 2nd order-filter.

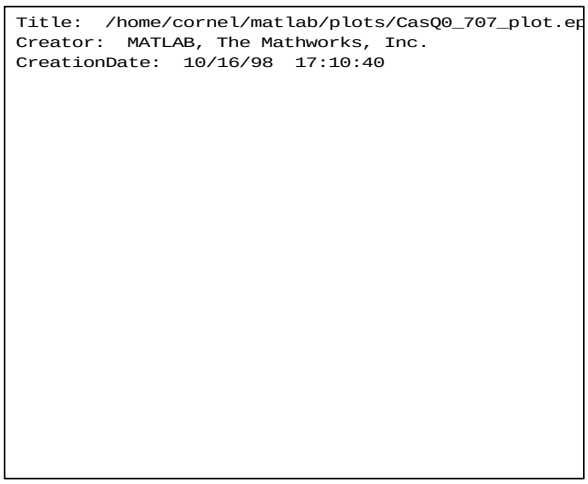

Figure 8. Settling behavior of cascaded filters (Q=0.707) from 2nd- up to 20th-order (lowest curve is one biquad, and successively highest is ten biquads).

This graph shows that the settling time of a system is, as in a 2nd-order system, proportional to the reciprocal value of the corner frequency and differs from filters of smaller order with an offset. This is analogous to the modeling of the settling time of 2nd-order systems. Additional measurements with different quality factors showed the same result with regard to the shape of the curve.

7. SYSTEMS WITH DOMINANT POLES

The model for the settling time of systems of 2nd order can be extended to systems of higher order with one pair of dominant poles (Nagrath 1975), that is one pair of poles very close to the imaginary axis. These dominant poles specify the

time response of the system as long as their real part is much smaller than that of the other poles. In that case the non-dominant poles can be neglected and the system can be approximated by a 2^{nd}-order system with respect to the settling behavior. The problem now is to find a minimum value for the ratio of non-dominant to dominant poles above which it is possible to handle the system as a biquad. Thus, measurements were done that vary the ratio of the real parts of non-dominant (all identical) to dominant poles. The variation of the poles was performed by choosing different corner frequencies, since the real part of the pole is proportional to the corner frequency of the appropriate biquad block. Figure 9 shows the results of the measurements of low pass (high-*Q*) filters of different orders, established by cascading biquads, with varying ratio (*R*) of the real parts of the non-dominant to dominant poles. The constant (lowest, straight) line in the graph represents the value for the settling time of the appropriate 2^{nd}-order filter.

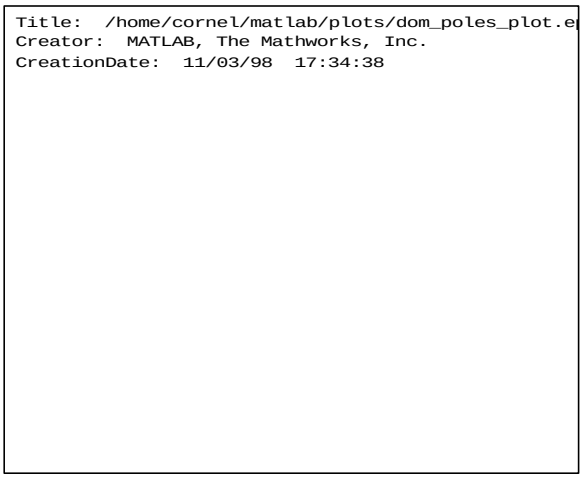

Figure 9. Settling behavior of systems with dominant poles (lowest, straight line - 2^{nd} order filter, highest line - 20^{th} order filter).

This graph shows that poles that are located close to the dominant pair have a high influence on the time response and increase the settling time significantly. This influence disappears above a minimum ratio of the real parts of non-dominant to dominant poles: R_{min}=4. Therefore, for systems with poles, whose real parts are much bigger that that of a dominant pair, the settling time of the system of higher order is almost equal to 2^{nd}-order system.

8. SUMMARY AND FUTURE WORK

This paper presents a model for dynamic reconfiguration of analog filters using 2 parallel Field Programmable Analog Arrays and switched multiplexer controlled by a digital system. Switching perturbations were analyzed and explained. In order to minimize the effects of these perturbations, analytical investigations about settling behavior of filters of 2^{nd} order were performed and a model for the transitions associated with a time delay of the switching after the reconfiguration process was established. It has been shown that this theoretical rule can be used for determination of the time delay, which is needed in optimization of the transition behavior during switching from one FPAA to another. The model for the time delay was confirmed by measurements of all types of biquad filters. Measurements of cascaded systems show that the behavior of the settling time with respect to changes of the characteristic values, the corner frequency and the quality factor, is analogous, to that of a biquad filter. The model was extended to systems of higher order with a pair of dominant poles, where it is possible to neglect the non-dominant poles and to handle the system as a 2^{nd}-order system. Using this model of the settling time it is possible to generate the proper time delay for the switching to obtain the output signal without undesired switching perturbations. For optimization of the multiplexing process and minimization of the effects of imperfections this model can now be used to implement a digitally controlled time delay into a FPGA, which replaces the controlling task of the PC and the switching part of the multiplexer. These experiments described here were performed to optimize the reconfiguration process in applications of adaptive filtering. However, the modeling results will be used in

constructing systems that support dynamically reconfigurable analog/digital hardware in general. More sophisticated and faster reconfigurable systems can be constructed using several FPAAs that are being reconfigured and switched by a FPGA. For each of the FPAA applications a specified time delay can be modeled and applied to the system in the form of a look-up table where the FPGA, selects the appropriate time delay. A block diagram of such a system is shown in Figure 10.

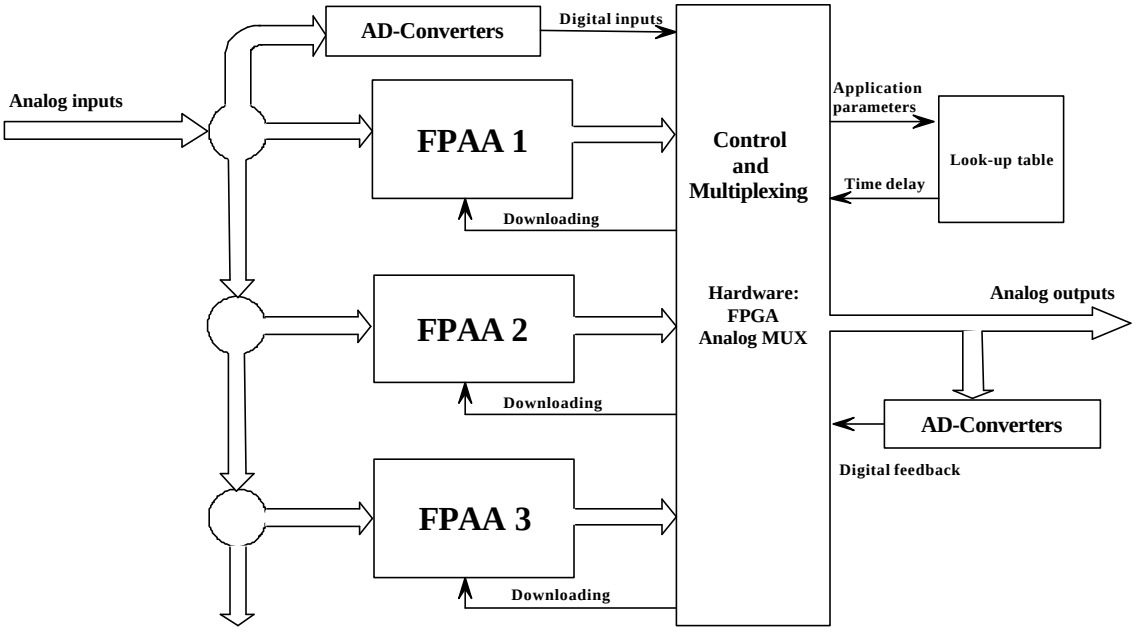

Figure 10. Block diagram of the system using a FPGA with a look-up table and blocks of programmable chips.

The time delay for an FPAA application is determined by proper parameters, such as the corner frequency and the quality factor at adaptive filtering. The FPGA provides the parameters for the reconfigured function and takes the appropriate time delay out of the table. Such system provides for a variety of different adaptive applications with optimized transition behavior.

ACKNOWLEDGEMENTS

This work was carried out at the Center for Low Power Electronics (CLPE) and was supported by the National Science Foundation, the Department of Commerce of the State of Arizona, and high-tech companies, members of CLPE. The membership includes Ambit, Analog Devices, Analogy, Burr Brown, Gain Technology, Intel, Inter-HDL, Microchip, Motorola, Raytheon, Rockwell, Texas Instruments, and Western Design.

REFERENCES

Birk, C. 1998. “Evaluation of Filters implemented using a Field Programmable Analog Array” Diego, California, Jan. 11-14, 1998.

Nagrath, I.J. 1975. *Control systems engineering*, John Wiley & Sons, New York

. *Journal of Circuits, Systems and Computers*. World Scientific Pub, Oct. 1998 (in print).

Weisberg, S. 1985. *Applied Linear Regression*, John Wiley & Sons, New York.

Znamirowski, L., O. A. Palusinski 1998. "Field Programmable Analog Arrays in Adaptive Filters Applications", *Reprogrammable Digital Systems, Proceedings of the I National Conference*, Szczecin, March 12-13, 1998 (in Polish).