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***OPTIMIZATION OF PERFORMANCE OF
DYNAMICALLY RECONFIGURABLE MIXED-SIGNAL
HARDWARE USING FIELD PROGRAMMABLE ANALOG
ARRAY (FPAA) TECHNOLOGY***

Diplomarbeit

von

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1. INTRODUCTION

1.1 Abstract

This work presents an investigation of a dynamically reconfigurable mixed-signal circuit using the new technology of Field Programmable Analog Arrays (FPAAs) combined with a digital system for control and reconfiguration of the analog circuits implemented on the FPAAs. A FPAA can be used to build filters for analog signals as well as other kinds of analog applications implemented in switched capacitor technology (S/C-technology). The experimental studies described in this work take advantage of the performance and programmability of the FPAA for filtering of an analog signal. The circuit structure is based on 2 parallel FPAA chips that are cooperating with a digital control system and are being switched by a multiplexer. Dynamic reconfiguration is used in this system for adaptive filtering, or analog processing in general. Theoretical studies and measurements of the transition behavior of the switching process between the two FPAA chips and the analysis of limitations imposed by hardware imperfections is presented. The experimental system is an excellent vehicle to learn about intricacies of the performance of mixed-signal circuits and is used for verification of theoretical predictions as well as for model modifications.

1.2 Background

Filters for processing data are essential components of contemporary electronic systems. Indeed, it is difficult to find even a moderately complex electronic device that

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does not contain one or more filters that are useful in many tasks. There exist four major types of filters that are presented and applied in this work. There is the class of *low-pass* filters that have the properties that low-frequency excitation signal components, even down to direct current, are transmitted while high frequency components, up from a characteristic value named *corner* or *cut-off frequency*, are inhibited and not visible in the output signal. The range of the passing (here: low) frequencies is called the *bandwidth* of the filters. By contrast, there is the class of *high-pass* filters that work just the opposite, that means the filter blocks the frequencies lower than a specified value and amplifies the higher components. The third type of filters is called *pass-band* filters and is characterized by one band of frequencies, the pass-band, where the frequencies are transmitted, while below and above this band, in the *stop-bands*, they are blocked. Conversely, there is the class of *band-stop* filter, where below and above the stop-band the frequencies are amplified while the frequencies in this specified band are cut-off. If this band is very narrow in order to inhibit one desired frequency, this filter is called *notch* filter and the blocked frequency is the *notch* frequency. Modifications and different implementations of these four basic filter types are applicable in many modern electronic circuits. Filters find many applications for example in the telecommunication area. The information signal that has to be transmitted is ‘modulated’ on a sinusoidal carrier signal, that is usually known as the ‘channel’ frequency by radio sets or clock radios. The carrier signal is detected and extracted off all the possible frequencies by frequency-selective filters. Digital circuits always need filters to avoid aliasing of frequency bands and to reconstruct the signal. Therefore both, analog and digital circuits, offer many applications for different filters. There are many ways to realize filters. Analog circuits offer the possibility to realize a filtering function in an active RC-circuit. However, these filters are fixed by their hardware components and cannot be changed like a digital filter implemented on a Field Programmable Gate Array (FPGA) which is capable of being reprogrammed. Both technologies, digital and analog circuits in general, offer advantages and disadvantages.

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Digital circuits can be used to implement high-accuracy and high-complexity signal processing algorithms for low frequency signals unless power dissipation during operation is critical. Analog circuits offer advantages in applications where signal frequencies are high and low power dissipation is essential. However, the accuracy of analog circuits is limited and they can not be used to implement algorithms of high complexity. Consequently, processing in a large system is assigned accordingly to analog and digital circuits to take advantage of their specific circuit properties for overall performance optimization, such as power minimization. As the complexity of modern processing systems grows, the traditional design of sophisticated functions, such as the strict separation of analog and digital functions, disappears more and more with modern design techniques. Additionally, it is desirable to create flexible systems in order to use them in diverse applications. If the processing requirements and algorithms change over time, the optimal assignment of processing functions may change and dynamic reassignment of functions and reconfiguration of circuits may be necessary. The technology of analog circuits did not provide so far the capability of changing the circuitry once it was built up. The new technology of Field Programmable Analog Arrays (FPAAs) in combination with a digital control system, such as the well-known technology of Field Programmable Gate Arrays (FPGAs), provides a basis for the development of a dynamically reconfigurable analog/digital hardware. Such a mixed-signal circuit is very suitable for applications in mobile systems, such as cell phones and other portable telecommunication systems in general, because power dissipation can be reduced by proper assignment of hardware processing functions to analog and digital circuits.

2. SWITCHED CAPACITOR (S/C-) TECHNOLOGY

2.1 *Basic concept*

Electrical signal processing systems are usually divided into two categories: analog and digital systems. An analog system carries signals in the form of continuous functions of the continuous time variable. By contrast, in a digital system each signal is represented by a sequence of numbers of discrete value. Also these numbers are the sampled values of the signal, taken at discrete time instances. Thus, the digital signal can be described as a variable that is discrete in time and magnitude. Since the processing of the digital bits is usually performed synchronously, a timing or clock circuit is an important part of the digital system. Digital systems can be used to implement high-accuracy and high-complexity signal processing algorithms for low frequency signals because of the limitations by its clock frequency whereas analog circuits offer advantages in applications where all kinds of signal frequencies are present.

The switched-capacitor (s/c-) technology of the circuits described in this thesis fall into a category which is in between the two main classifications described above. This is the category of sampled-data analog systems where the signal is represented by a continuous amplitude of an electrical quantity but only at discrete time instances, as in a digital system. Such a circuit can be fabricated utilizing standard digital MOS technology, and hence can also be placed on the same chip with digital circuitry. This latter aspect is of great importance for example in telecommunication systems, where both analog and digital functions are needed within the same functional block.

SWITCHED CAPACITOR (S/C-) TECHNOLOGY

Consider the simple analog transfer function in the s-domain, defined by the division of the output voltage by the input voltage of the analog circuit:

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{b}{s^2 + as + b}, \quad (2-1)$$

where a and b are constant values. The s-domain can be derived by using the Laplace-transformation, where time functions (here: $h(t)$) are mapped into the complex s-domain with the independent variable $s = a + j\omega$.

It is easy to verify that a circuit with typical electrical components, such as resistors (R), inductance (L) and capacitors (C), can realize this function. While such a circuit is easy to design, build and test, the presence of an inductor in the circuit makes the manufacturing in an integrated circuit impossible because of its oversize and insufficient accuracy. To overcome this problem, the designer may decide instead to create the desired transfer function using an active RC-circuit which utilizes operational amplifiers. This circuit needs no inductors and may be realized with small-sized discrete components. But a major problem of this circuit is the large chip area needed for all the RC-components and also the temperature induced variations and fabrication inaccuracies of the resistive and capacitive elements. An effective strategy to solve both, the area and the matching problems, is to replace each resistor in the circuit by a combination of a capacitor and a few switches who are changing dynamically between the signal paths and earth ground.

2.2 S/C-resistors

Consider the branch shown in Figure 2-1.

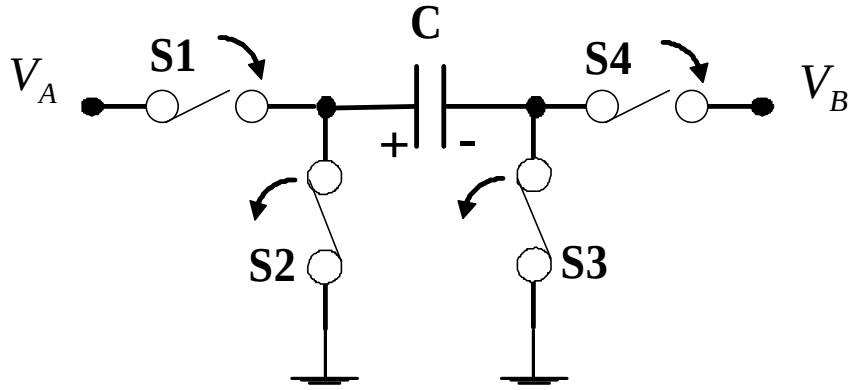


Figure 2-1 S/C-realization of a resistive branch

Here, the four switches S1, S2, S3, and S4 open and close periodically. The switches S1 and S4, as well as S2 and S3, operate synchronously but in the opposite phase. Therefore, when S1 and S4 are closed and S2 and S3 are open, C is charged to the voltage $V_C = V_A - V_B$. In the next phase, when S2 and S3 are closed, C is discharged. This process repeats periodically with the clock period T and therefore the changing charge

$$q = C[V_A - V_B] \quad (2-2)$$

represents an average current

$$i = \frac{q}{T} = \frac{C}{T}[V_A - V_B] \quad (2-3)$$

through the branch.

SWITCHED CAPACITOR (S/C-) TECHNOLOGY

Therefore, the branch can be replaced by an equivalent resistor

$$R = \frac{T}{C}. \quad (2-4)$$

In order to determine the correct value of a resistor both variables, the capacitor size C and the clock time T , have to be specified.

The two phases of the clocking are illustrated in Figure 2-2. In the first phase Φ_1 only switches $S1$ and $S4$ are open and in the second phase Φ_2 only $S2$ and $S3$.

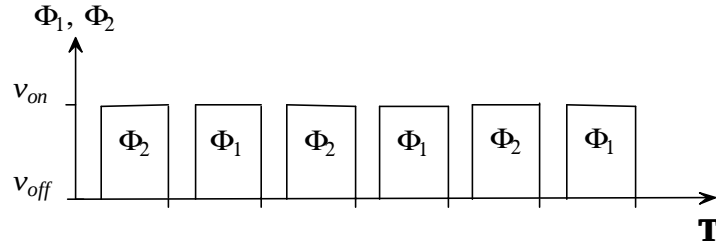


Figure 2-2 Two phase clocking scheme used in S/C circuits

2.3 Second-order analog filters

A biquadratic filter transfer function, simplified called 'biquad', is usually expressed in the form:

$$H_{biquad}(s) = -\frac{K_2 s^2 + K_1 s + K_0}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}, \quad (2-5)$$

SWITCHED CAPACITOR (S/C-) TECHNOLOGY

where the filter characteristics are specified by the constant parameters K_2 , K_1 , K_0 , w_0 , and Q . The symbol w_0 represents the corner frequency in rad/s and Q is the quality factor of the filter, both associated with the complex poles $s_p = \sigma_p \pm j\omega_p$ of $H_{biquad}(s)$, where σ_p is the real part and ω_p the imaginary part of the complex value of s_p as shown below:

$$w_0 = \sqrt{\sigma_p^2 + \omega_p^2} \quad (2-6)$$

and

$$Q = \frac{1}{2} \sqrt{1 + \left(\frac{\omega_p}{\sigma_p}\right)^2}. \quad (2-7)$$

These two characteristic values describe the frequency behavior of the filter response. If Q is high (say 10 or more) the pole, that can be achieved by setting the denominator of the transfer function to zero, is relatively close to the $j\omega$ -axis in the complex s -domain, and it causes $H_{biquad}(j\omega)$ to have a sharp peak near w_0 in the frequency response. Such functions tend to have widely spread element values, and higher sensitivity to element-value variations near w_0 .

This transfer function can be realized in the active-RC circuit using operational amplifiers (OP) shown in Figure 2-3.

SWITCHED CAPACITOR (S/C-) TECHNOLOGY

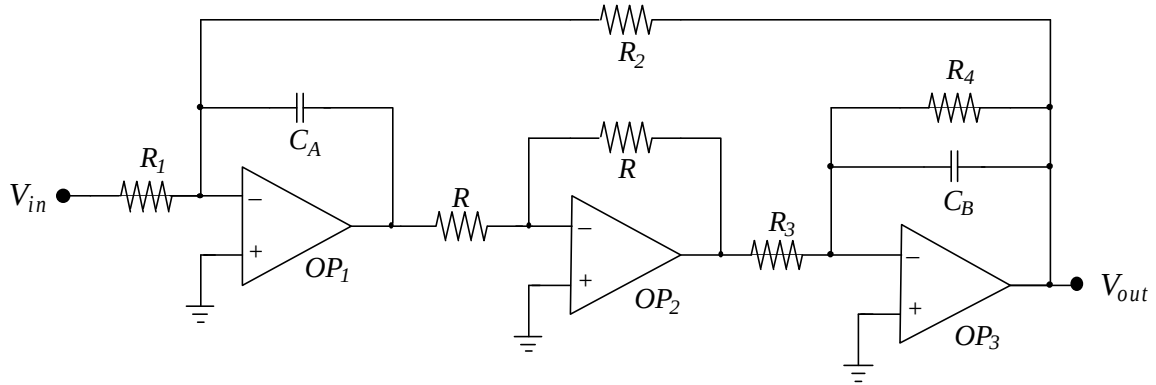


Figure 2-3 Active RC-realization of a filter of 2nd order

It is plausible that all resistors in Figure 2-3 can be replaced by the S/C-branch shown in Figure 2-1. The resulting circuit is illustrated in Figure 2-4:

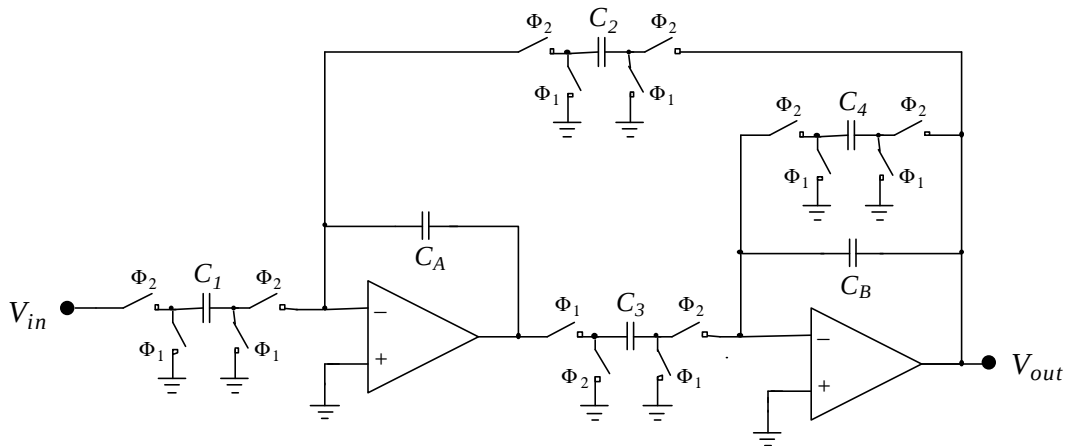


Figure 2-4 S/C realization of filter of 2nd order

A major advantage of this new arrangement is that all time constants, previously determined by the inaccurate RC-components, are all determined by a product of the

SWITCHED CAPACITOR (S/C-) TECHNOLOGY

clocking time and a capacitor ratio. Since the clock period is generated by a quartz-crystal-controlled clock circuit, the clocking is very accurate and stable. The other factor of the time constant, a ratio of two on-chip MOS capacitors, can also be established with high accuracy and stability using some simple rules in the layout.

Another improvement is the reduction of required chip area using s/c-technology. When very short time constants are needed, such as in audio-frequency applications, very large resistors around several $M\Omega$, are required that occupy a prohibitively large part of the entire chip area. By contrast, at a typical clock frequency of $100kHz$ the capacitance of the switched capacitor realizing a $10M\Omega$ -resistor is $1pF$. This capacitor requires only 0.25% of the area needed by the resistor which it replaces. Using the three types of components, operational amplifiers (op-amps), capacitors, and switches, a large quantity of analog signal processing circuitry, such as filters, analog-to-digital and digital-to-analog converters, gain amplifications, as well as nonlinear operations as multiplication, modulation, detection, rectification and others, can be placed on a single chip.

The second operational amplifier (OP_2) of Figure 2-3 acts mainly as a phase inverter and has been eliminated in the s/c-realization of the filter. This was possible since by simply changing the phasing of two of the four switches associated with the capacitor C_3 , the phase inversion could be accomplished without an op-amp. The same circuit of Figure 2-1 can be used but with clock phases shown in Figure 2-5. With this phasing, a positive V_A will result in negative charges being delivered to the op-amp, just as in a negative resistor. With the phase inversion and the required capacitor size of $C = \frac{T}{|R|}$ it is possible to realize this negative resistor in s/c-technology.

SWITCHED CAPACITOR (S/C-) TECHNOLOGY

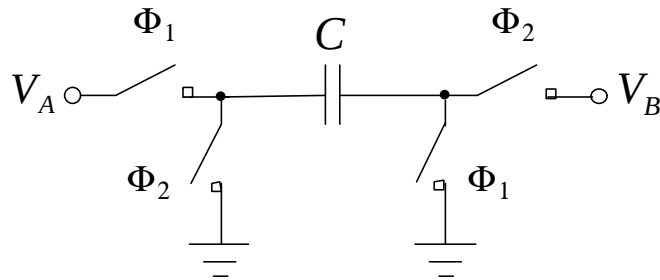


Figure 2-5 **Negative resistor in S/C-technology**

2.4 Switch sharing

By close examination of Figure 2-4 it can be recognized that there are some switches that can be used jointly by different branches. This technique, called switch sharing, simplifies the development of the circuit and can optimize the utilization of the chip area.

The circuit of Figure 2-6 illustrates the simplification resulting from switch sharing.

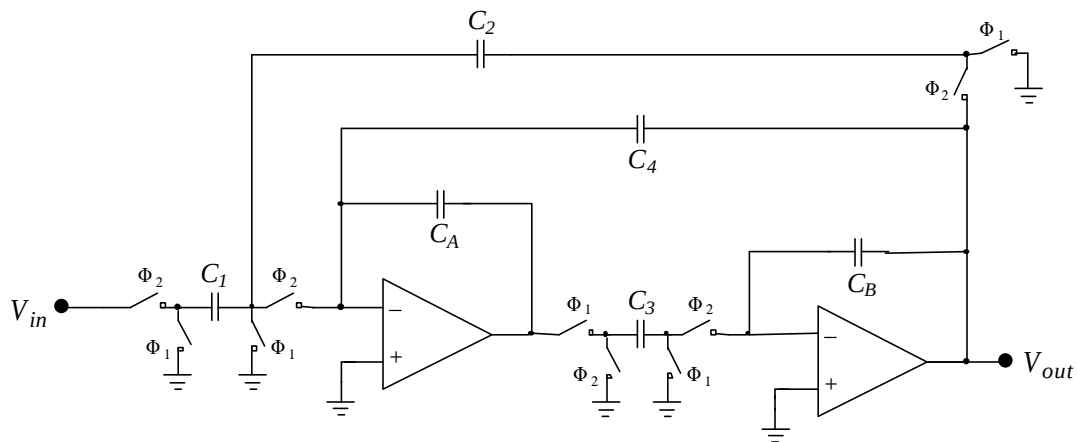


Figure 2-6 **Switch sharing applied to a 2nd-order filter**

SWITCHED CAPACITOR (S/C-) TECHNOLOGY

The basic results described in this chapter are drawn from the fundamental monograph on CMOS switched capacitor circuits and technology by Gregorian and Temes [Gregorian 1986].

3. THE FIELD PROGRAMMABLE ANALOG ARRAY

3.1 MOTOROLA's MPAA020

The new technology of Field Programmable Analog Arrays, built in CMOS technology, is a very suitable device for realizing different analog circuits based on the S/C-concept. It can be used for numerous engineering applications like electrical signal filtering, construction of controllers, phase correctors for continuous and sampled data feedback systems, and signal generation. The power of the FPAA is that it is an ideal device for quick reconfiguration due to its software support allowing for easy design, debugging and implementation of various analog functions. The chip is divided into 20 identical, uncommitted, configurable analog blocks (CABs), each with one operational amplifier, five capacitor banks and diverse switches as illustrated in Figure 3-1. Four of the capacitor banks are located between the internal routing block and the switches and one capacitor bank is in the feedback loop of the op-amp. On the left side there are diverse input stages entering the switch blocks and on the right side are the outputs of the CAB.

THE FIELD PROGRAMMABLE ANALOG ARRAY

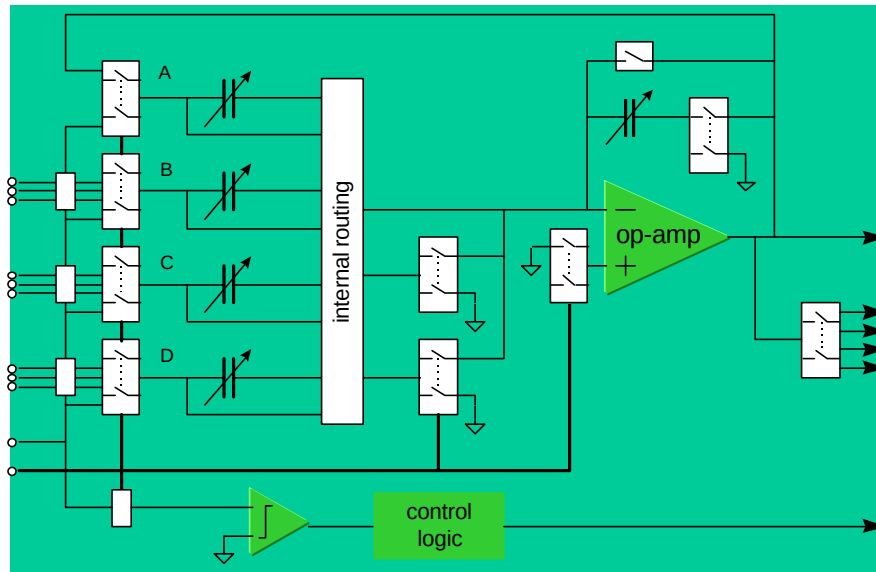


Figure 3-1 Programmable analog block (CAB) of the FPAA

There are static switches forming the connections between the diverse components within the block and dynamic switches that represent, in combination with a capacitor, a resistive function. In order to determine the processing function the static switches are set once during the programming phase of the chip, after which they remain unchanged. The dynamic switches are switched periodically by the internal clock frequency during the circuit operation in order to change the charges of the capacitors as typically done in s/c-circuits. Additionally, there are switches that allow limited connection to be made between components of two CABs that are located close to each other within the chip. There are also 'global wires' on the chip that allow connections between CABs that are far apart. The chip contains 41 operational amplifiers, 100 programmable capacitors, 6864 electronic switches, and 13 input/output buffers. The whole array is structured in a grid that contains the 20 blocks established in a 4x5 matrix as illustrated in Figure 3-2 .

THE FIELD PROGRAMMABLE ANALOG ARRAY

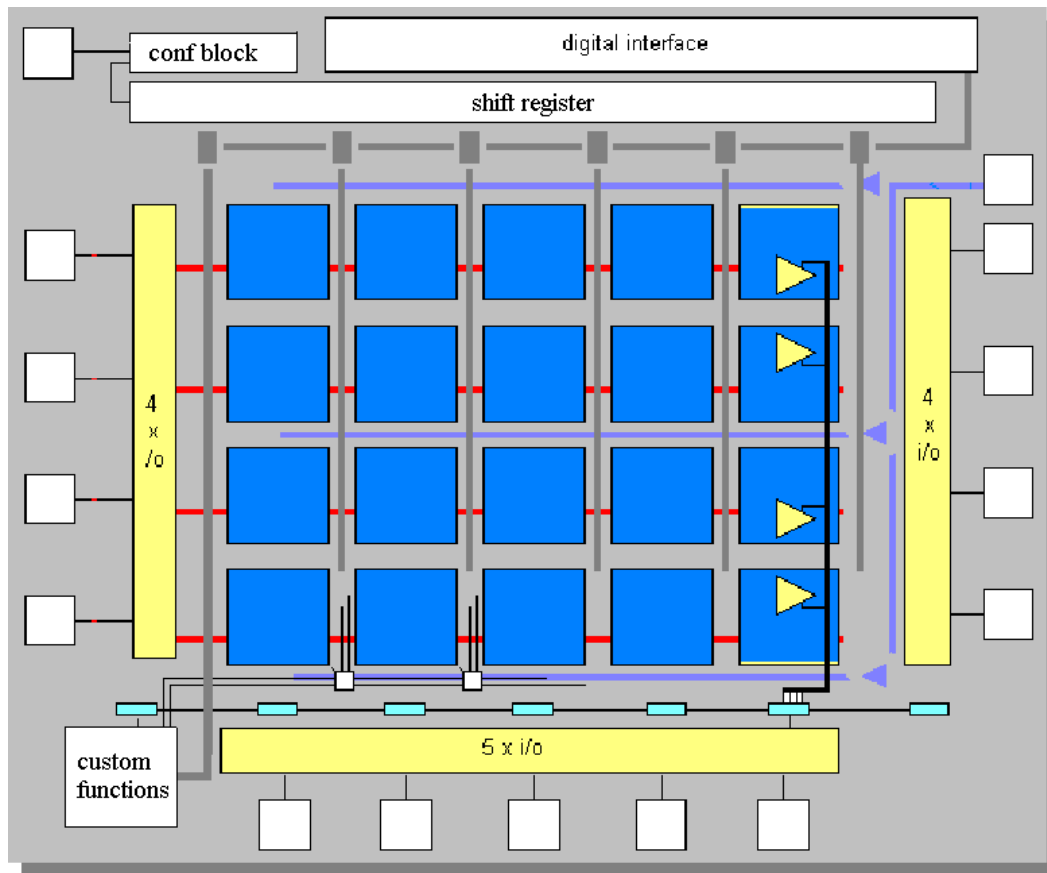


Figure 3-2 Block diagram of the FPAA

3.2 The Software *EasyAnalog*TM

The complexity of control of the chip is so high that a software, called *EasyAnalog*TM, was developed to support the programming of the chip. Configuration of an analog circuit on the chip is performed by downloading a 6K data stream via RS232 communication from a digital system. The software creates the data that determines the required switch settings

THE FIELD PROGRAMMABLE ANALOG ARRAY

and capacitor sizes in order to generate the desired analog function and downloads the data into a *619 bit* wide shift register on the chip. During the configuration phase all CABs are set into a power-down mode to protect the array against undesirable high currents. The software runs under Windows 3.1, Windows 95, and Windows NT operating systems. A graphical interface, shown in Figure 3-3, shows a simplified view of the 20 CAB arrangement on the chip and makes it easy for a user to realize a desired analog processing function.

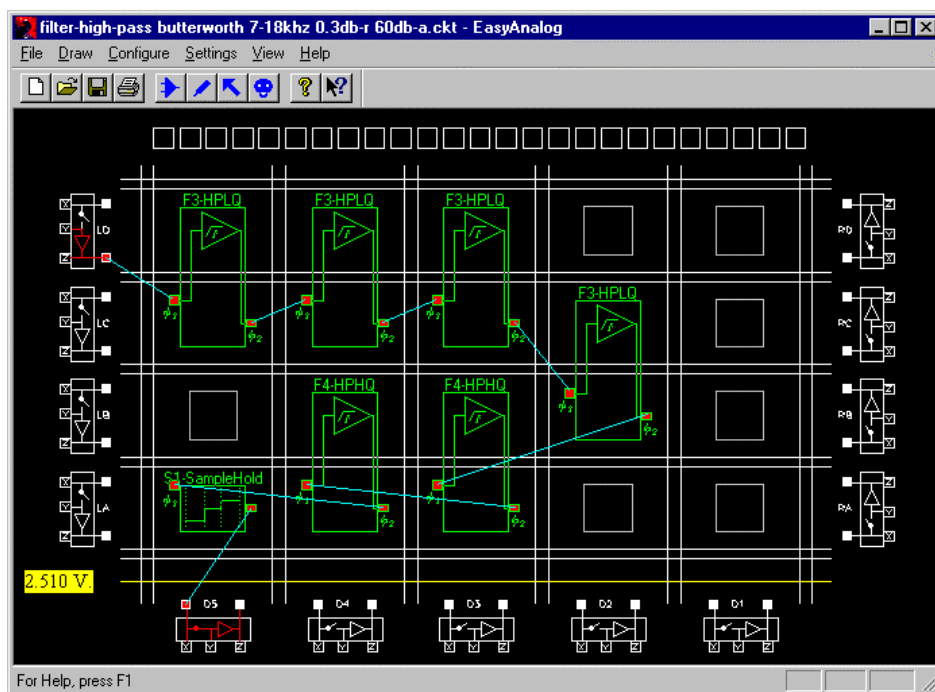


Figure 3-3 CAD Interface of EasyAnalog™

With a ‘point and click’-action the user can select pre-defined ‘macros’ from a function library and place them onto the chip as desired. The macros can be ‘wired’ together by a ‘drag and drop’-action. However, there are also diverse pre-configured circuits saved in a library that can be used for diverse applications. The parameters of a chosen or configured circuit can be set using pull-down menus and pop-up windows. This makes it easy for an

THE FIELD PROGRAMMABLE ANALOG ARRAY

user to change characteristic values of a circuit, e.g. changing the corner frequency of a filter. The realized values may be slightly different from the desired values because of technological constraints, limited range of quantized values of the capacitors, and switching frequency limitations.

3.3 The Software Macro Editor™

A second software, called Macro Editor™, allows for the design and development of macros within one analog block (CAB) of the chip as shown in Figure 3-4. The established macros can be added to the libraries of EasyAnalog™. The software is still in development and is not yet very sophisticated. Not all features of the chip are available and faulty circuits can be unintentionally developed without warning because the software does not have any extensive error check routines.

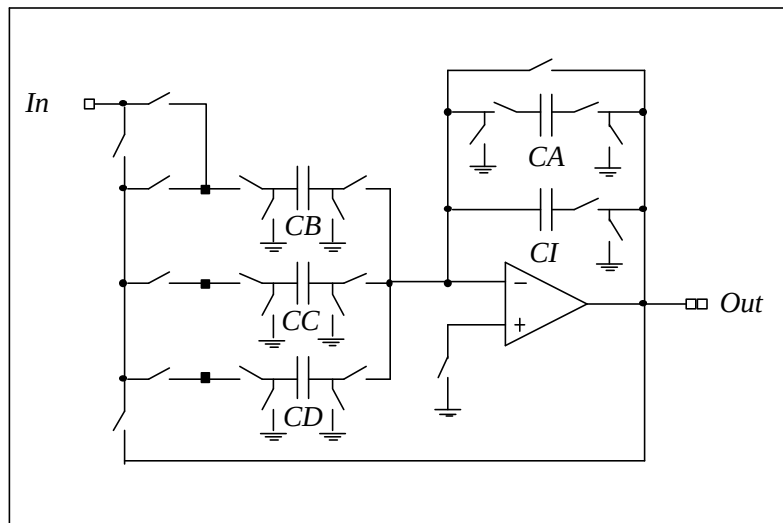


Figure 3-4 Single CAB as displayed in Macro Editor™

3.4 Additional features of the chip

The chip contains additionally a voltage reference wire that can be set to one of 256 voltage values using a setting dialog window in EasyAnalog™. The desired I/O- (input/output) stage of the chip can be selected and the signal can be wired to all locations on the chip using horizontal and vertical ‘global’ wires. An internal anti-aliasing filter is also available. The capacitor banks are structured in the form of a matrix of capacitors of unit size. The desired capacitive value is realized by using a matrix of unit capacitors connected in parallel. The parameters of an analog transfer function are generated by a ratio of capacitors and therefore there is no need for unnecessary high physical values of the electrical components. However the fact that only the implementation of integer multiples of the unit capacitor size is possible leads to quantization errors [Palusinski 1998, Birk 1998].

Normally, the signal ground for the MPAA020 is set up to 2.5V as generated internally to the chip and an analog range is running from 0V up to 5V. The evaluation board contains a 1MHz clock, a 5V power supply, a serial EPROM in order to store configuration data, and an anti-aliasing filter of 4th order for up to 200kHz.

This and other characteristics of the MPAA020 are presented in [MOTOROLA 1997].

4. DYNAMIC RECONFIGURATION

4.1 Concept

The basic concept of a dynamically reconfigurable mixed-signal hardware is demonstrated here by using 2 parallel FPAA's, which are being switched by a multiplexer, and a digital system, which controls the switching and provides the communication to the FPAA's in control of reconfiguration. In this thesis all the control is done manually using a PC and the software EasyAnalog™ to perform initial studies whose results are essential for future incorporation of Field Programmable Gate Array (FPGA) technology. Digitization of the analog signal input and output to the FPGA is also planned in order to implement a digital feedback loop for comparison and control of the desired filter behavior. The current experimental setup is established without the feed-back and feed-forward loops and is primarily intended to be used for investigations about switching inaccuracies and performance imperfections caused by the hardware. A more sophisticated control system, implemented on FPGA, could analyze the input signal and generate the desired filter function. However, the realization of the multiplexer and of the software for control of the whole system into a FPGA is beyond of the scope of this work and is being investigated as a different project. Chapter 10.2 illustrates the future plans in more detail what could have to be done. The block diagram of the system is shown in Figure 4-1.

DYNAMIC RECONFIGURATION

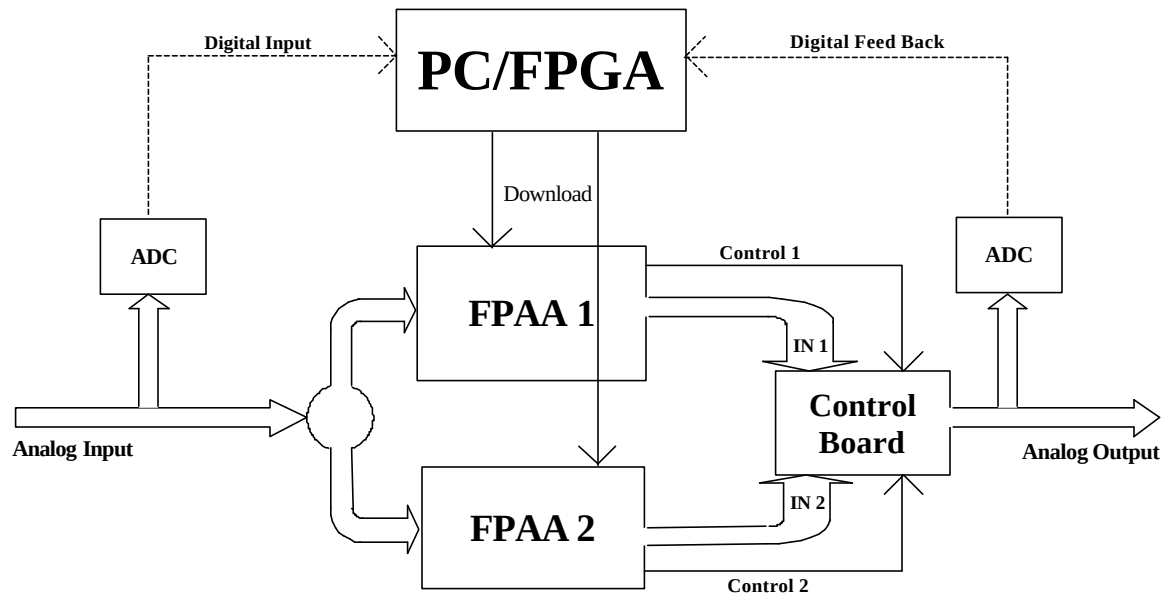


Figure 4-1 Block diagram of the system composed of 2 parallel FPAA's

A control signal for the multiplexer on the control board is generated on the FPAA during the programming phase. So when the FPAA starts to work after reconfiguration a logic 'HIGH'-signal appears at an specified output pin of the FPAA that enters into an adjustable time delay circuit and then into a multiplexer on the control board in order to interchange the analog outputs of the FPAA's. The time delay circuit is established in order to have the possibility of a time lag between the end of the reconfiguration phase, when the FPAA starts processing the input signal, and the physical switching of the multiplexer to the output of the reconfigured FPAA.

In this system one FPAA can filter the analog input signal while the second one is 'off-line' waiting for reprogramming. After its reconfiguration the multiplexer switches from the first FPAA to the reconfigured FPAA and then the other one is capable to be reprogrammed. With this system it is possible to change the filter characteristics while processing in order

DYNAMIC RECONFIGURATION

to provide the desired output signal behavior. The system using 2 FPAAs provides a steady output signal without interruption when redefinition of the analog filter function is needed, such as changing the quality factor or adjusting the corner frequency. The described process is illustrated in the timing diagram in Figure 4-2.

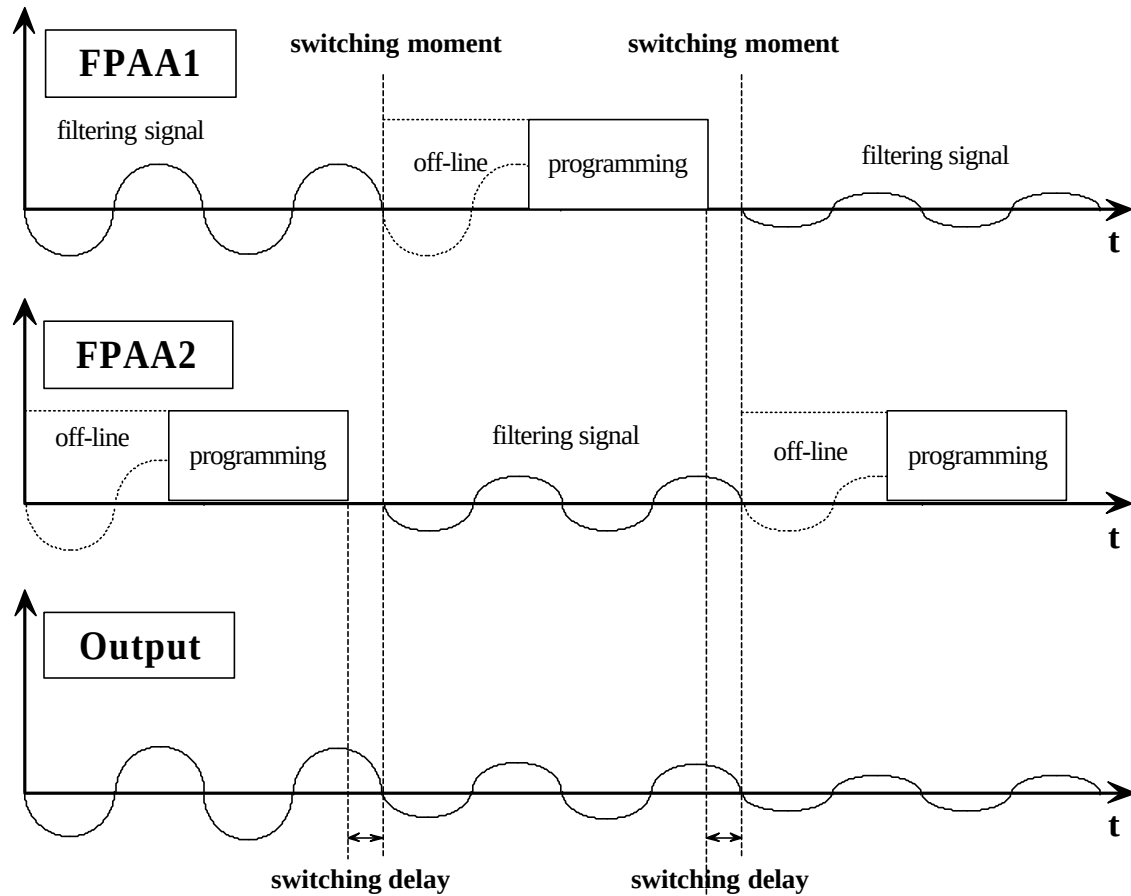


Figure 4-2 Timing diagram of reprogramming and filtering of 2 parallel FPAAs for uninterrupted processing of an analog input signal

DYNAMIC RECONFIGURATION

A complicating factor of the dynamic reconfiguration is the transition behavior of the switching from one FPAA to the other. After the FPAA is reprogrammed it cannot be put immediately ‘on-line’ because the signal needs some time to settle and reach a steady state. That’s why it is necessary to provide a time delay between the end of the programming phase and the actual switching. The switching perturbations are discussed in more detail in chapter 5.

4.2 The control board

The main problem of designing the hardware for the multiplexer is to establish the previously mentioned adjustable time delay device for the control signal. Two dual retriggerable monostable multivibrators 74123 (U5, U6, U8) built up in series, were used for this purpose. An output pulse can be terminated by a LOW-going edge on the specified trigger input pin, which also inhibits the triggering. The output pulse width is determined by the selection of an external resistor (***R1,R2***) and capacitor C_{ext} . For $C_{ext} < 10nF$ there is a defined basic output pulse whose width cannot be reduced, but for $C_{ext} > 10nF$ the length of the pulse is defined as:

$$t_w = 0.45 * R_{ext} * C_{ext} \quad (4-1)$$

where t_w is the pulse width in *ns*, R_{ext} the external resistor in $K\Omega$, and C_{ext} the external capacitor in *pF*.

Schmitt-trigger action in the inputs makes the circuit highly tolerant of slower input rise and fall times [PHILIPS 1997]. Using two of these devices in series, one with a HIGH-, the other with a LOW-output pulse, it is possible to create a time delay of the input signal that

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can be adjusted by potentiometers (**R1,R2**). The schematics of the entire circuitry is shown in Figure 4-3. The components of the system are specified in Table 1.

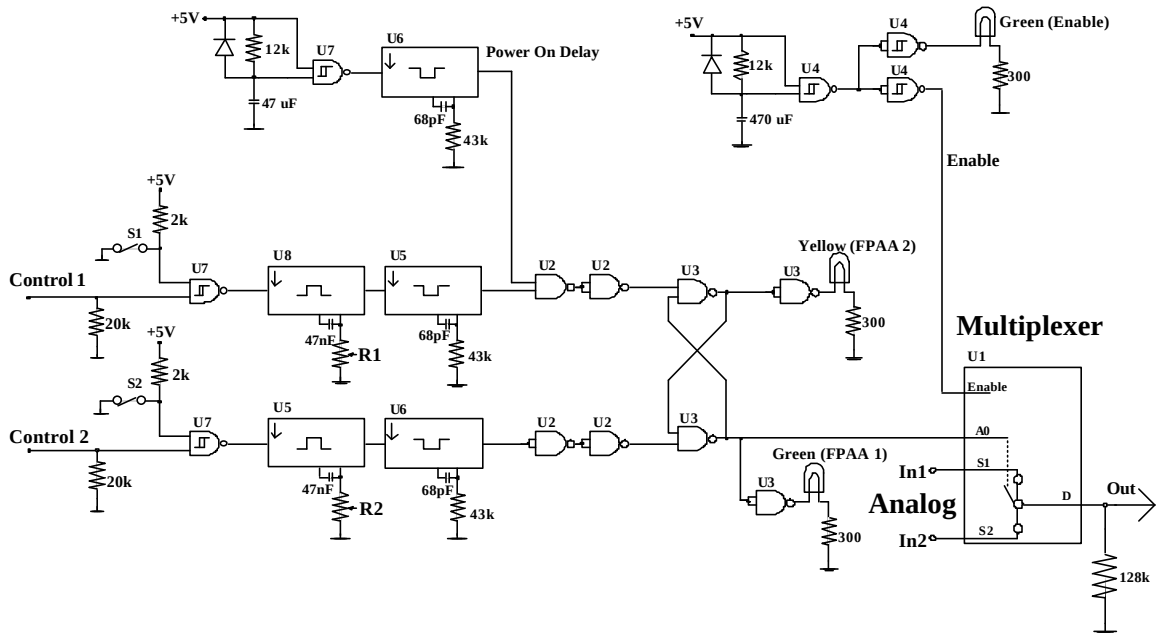


Figure 4-3 Schematics of the control board

Table 1 **Devices used in the control board**

U₁	DG 406 Multiplexer
U₂, U₃	7400 Quad 2-Input NAND Gate
U₄	74132 Quad 2-Input NAND Schmitt trigger
U₅, U₆, U₈	74123 Retriggerable monostable Multivibrator
U₇	74HCT132 Quad 2-Input NAND Schmitt trigger

DYNAMIC RECONFIGURATION

One of the Quad 2-input NAND-Gate 7400, noted as U3, creates the flip-flop, which controls the bit for the address pin A_0 of the multiplexer U_1 . In order to provide a stable process of the flip-flop, a basic minimum pulse width of the multivibrators 74123 (U5, U6, U8) was established at approximately $15\mu s$ by adjusting the appropriate values of the potentiometers as required by (4-1). The DG406 is a 16-channel single-ended analog multiplexer designed to connect one of sixteen inputs to a common output as determined by a 4-bit binary address. An enable function allows resetting the multiplexer, but this input is connected to the power supply of the whole circuit and equipped with a indicator LED . All control inputs, address pins and the enable input are TTL compatible over the full specified operating temperature range. Applications for the DG406 include high speed data acquisition, audio signal switching and routing. High performance, fast transition times, typically $200ns$, and low power dissipation make the multiplexer ideal for the experimental investigations [TEMIC 1997].

The control board includes three indicating LEDs, a green one for the enable signal that is on when the power supply for the circuit is on, and two for the control signals. These two LEDs are changing frequently according to the switching from one FPAA to the other. So with the yellow LED on the FPAA2 is connected to the output and FPAA1 is 'off-line', and vice versa with the green LED on. The circuit also includes a power on delay branch that divides logically the control signals from the flip-flop in order to provide a stable signal for a short time period right after the board is connected to the power. All the inputs have Schmitt-trigger gates for stabilization. The switches (S_1/S_2) are established for test tasks to enable the user to switch the input signal to ground if desired.

The circuit was developed on a breadboard with in the trade available devices on soldered sockets. The functions of the diverse chips are discussed closer in chapter 11.1.

5. SWITCHING PERTURBATIONS

5.1 *Settling behavior*

During programming of a FPAA the chip is reset and all capacitors are discharged. The output is also set to earth ground in contrast to the signal ground of 2.5V established on the chip. So when the programming is finished and the reconfigured chip starts to work there is the analog input signal added on a step function entering the circuit. A step function is a signal whose value changes from one constant level, usually zero, to another level A in zero time. This constant offset is established by setting to signal ground of 2.5V. Therefore the transition behavior can be treated as a step response of a system of second order with typical exponential settling behavior as discussed in detail in chapter 7. The circuit will be analyzed using sinusoidal analog input signals with small amplitudes as typically used in data processing applications. The sinusoidal signal is added to the constant offset of the internal signal ground and therefore in the output signal superimposed onto the shape of the step response established by the signal ground. A typical example of a measurement performed using a sinusoidal input signal is given in Figure 5-1. The lower curve represents the input signal and the upper curve shows the output signal with the switching process and settling behavior on the left side of the graph.

SWITCHING PERTURBATIONS

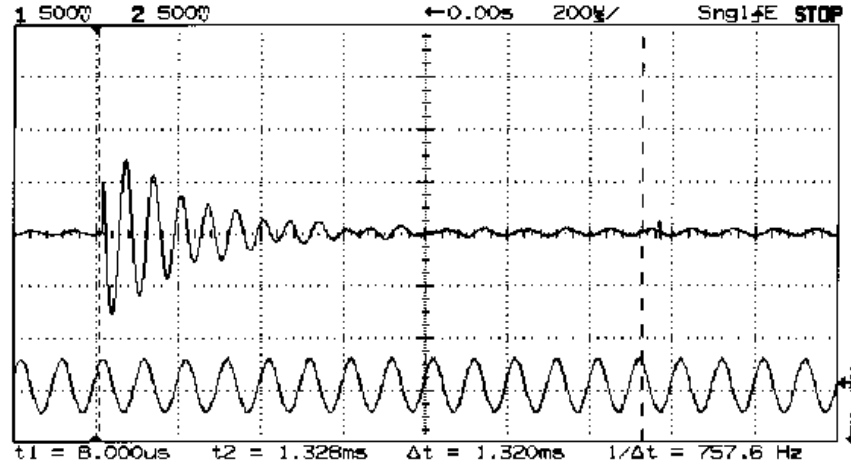


Figure 5-1 Settling behavior of a system of 2nd order after switching; the lower plot is the input signal and the upper plot the output signal.

To avoid the undesired settling behavior in the output signal a time delay is used for the control signal after the end of the programming phase, such that the physical switching is taking place right after the settling time of the signal. For better determination of the settling time a constant step function as the input signal was utilized during measurements.

5.2 Zero-crossing

Another important aspect of the switching process is the moment of switching within the period of the sinusoidal input signal. For example, if the user changes the quality factor of a low-pass filter of 2nd-order and switches at the peak of the sinusoidal input signal, there

SWITCHING PERTURBATIONS

will be a jump in the output signal as illustrated in Figure 5-2. Such jumps can happen during reconfiguration of filters in general.

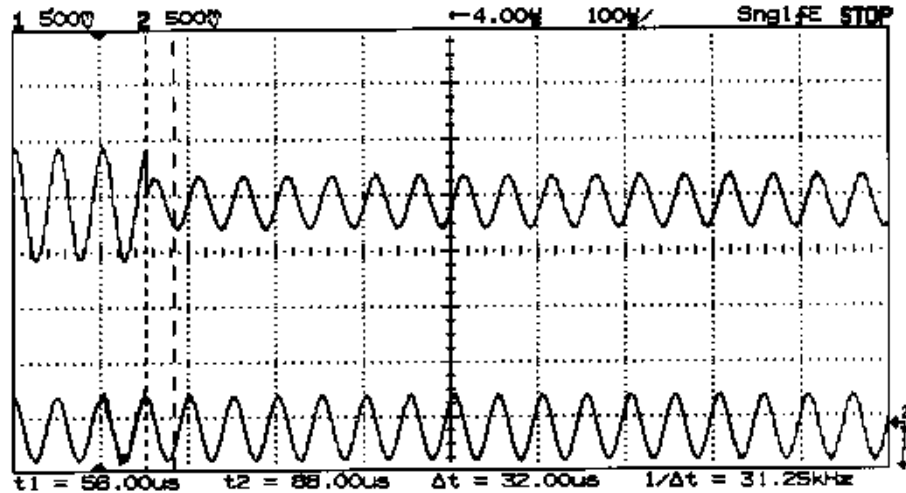


Figure 5-2 Amplitude jump caused by switching at the peak of the input signal; the upper curve is the output signal and the lower the input signal

Such a jump causes an injection of high frequency components that should be avoided using a low-pass filter as well as other filter implementations. Therefore it is necessary to switch at the zero-crossing of the sinusoidal input signal to minimize undesirable jumps of the amplitude. However, if the corner frequency of the filter or the whole filter in general will be changed, then the user has to deal with discontinuities in the amplitude as well as a phase shift. Some optimization may have to be used to determine the switching moment.

Figure 5-3 illustrates a requested switching transition at the zero-crossing of the signal. The lower curve is the input while the upper is the output signal.

SWITCHING PERTURBATIONS

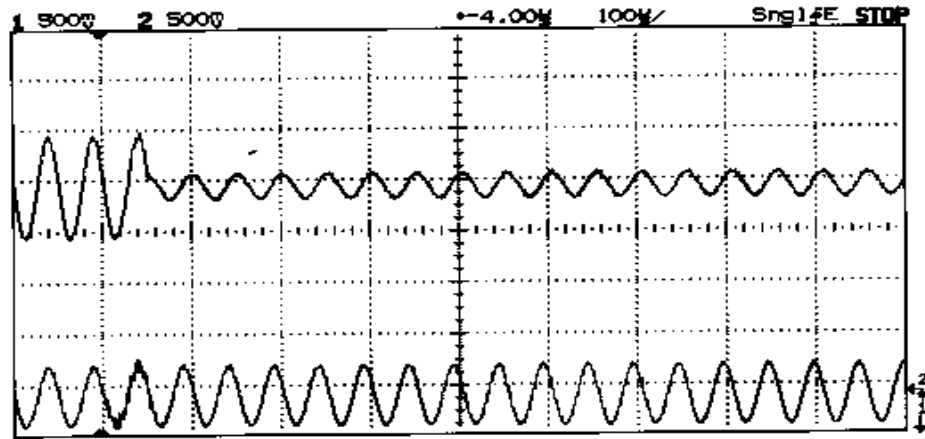


Figure 5-3 Switching at zero-crossing; the upper curve is the output signal and the lower the input signal

When the control system is implemented on a FPGA and a digital forward and backward loop is established, the input signal will be analyzed with regard to zero detection in order to switch exactly at the zero-crossing right after the time delay when signal is settled in.

6. FILTERS IMPLEMENTED ON THE FPAA

6.1 Filters of 2nd order in general

This chapter describes the development of a filter structure for implementation on a FPAA. The general transfer function of a filter of 2nd order is described by the form:

$$H_{biquad}(s) = -\frac{K_2 s^2 + K_1 s + K_0}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}, \quad (6-1)$$

where K_0 , K_1 , K_2 , ω_0 , and Q specify the filter characteristics. The corner frequency ω_0 , at which the peak of the magnitude response occurs, and the quality factor Q are the primary factors that describe the frequency-selective nature of the transfer function. The quality factor Q is defined as $Q = \frac{\omega_0}{3dB-BW}$, where $3dB-BW$ is the bandwidth defined as the difference between the corner frequency ω_0 and the frequency at which the transfer function magnitude is 3dB down from its peak magnitude [Huelsman 1980]. These second-order sections are often called biquads. This is a well-known transfer function and there is a substantial quantity of information in the literature on the active-RC realization of transfer functions of this form [Tietze 1991], [Giacoletto 1977], [Sedra 1991].

To obtain the block diagram of a system which realizes $H_{biquad}(s)$, we transform (6-1) into

$$s^2 V_{out} = -[K_2 s^2 + K_1 s + K_0] V_{in} - [\frac{\omega_0}{Q} s + \omega_0^2] V_{out} \quad (6-2)$$

FILTERS IMPLEMENTED ON THE FPA

Dividing both sides by s^2 and rearranging (6-2) leads to

$$V_{out} = -\frac{1}{s} \left[K_1 + K_2 s \right] V_{in} + \frac{w_0}{Q} V_{out} - w_0 V_1, \quad (6-3)$$

where V_1 is defined as

$$V_1 = -\frac{1}{s} \left[\frac{K_0}{w_0} V_{in} + w_0 V_{out} \right]. \quad (6-4)$$

V_1 can be obtained by integrating the weighted sum (6-4) of V_{in} and V_{out} , and V_{out} by integrating the weighted sum (6-3) of V_{in} , V_{out} , and V_1 . Therefore, a block diagram for the system can be build up using inverting integrators to provide the $-1/s$ -operations and diverse feedback and feedforward branches to provide the coupling of the diverse signals. V_1 can be obtained at the output of the first integrator. The resulting block diagram is shown in Figure 6-1.

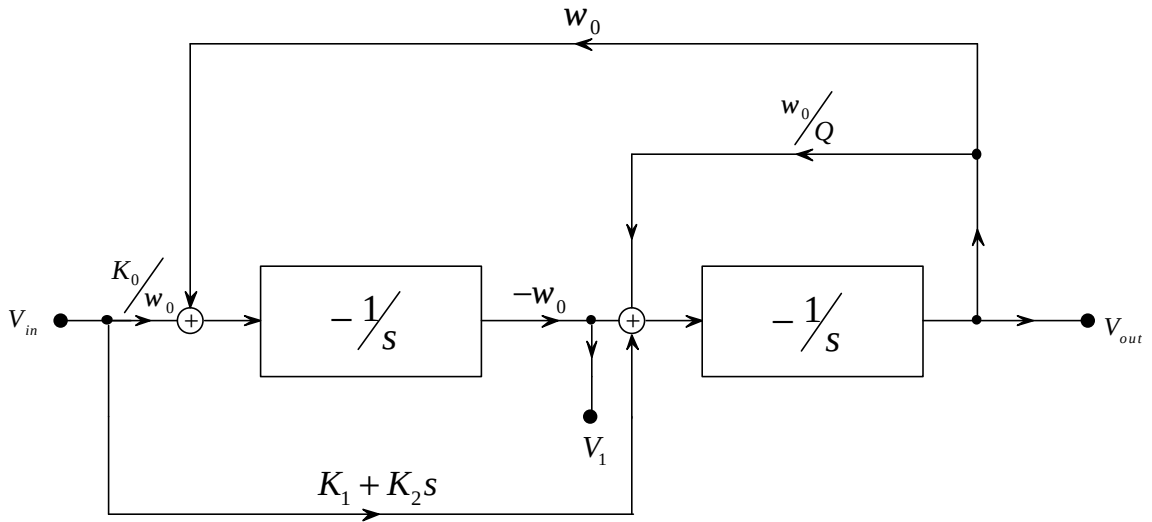


Figure 6-1 Block diagram of second-order filter

FILTERS IMPLEMENTED ON THE FPA

Assuming that the input signal of an integrator is a current and the output a voltage, the inverting integrator can be set up as an operational amplifier with a feedback capacitor (with a unit value of 1u) as it is typically done in analog circuits. The branches have the op-amp output voltages as input signals and as output signals the currents that are entering the integrators. Therefore a branch can be described with the transmittance $G = I_{out}/V_{in}$.

The transmittance shown in Figure 6-1 can be replaced by its reciprocal values and thus the analogous resistors for every branch of the equivalent electrical circuit are obtained. This filter can be realized in active-RC technology and is illustrated in Figure 6-2.

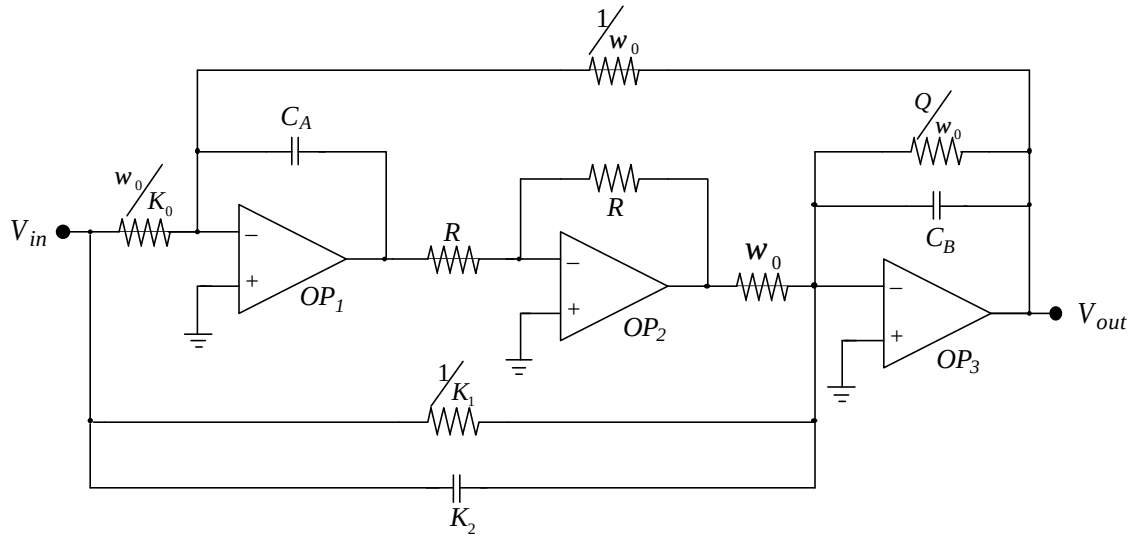


Figure 6-2 Second-order filter established in active RC-technology

The operational amplifier OP_2 in Figure 6-2 works as a phase inverter and can be replaced by a 'negative' s/c-resistor realized just by changing the clock phases of the switches as discussed in chapter 2.3. Replacing all resistors in this circuit by switched capacitors with adequate values yields the equivalent s/c-circuit shown in Figure 6-3.

FILTERS IMPLEMENTED ON THE FPAF

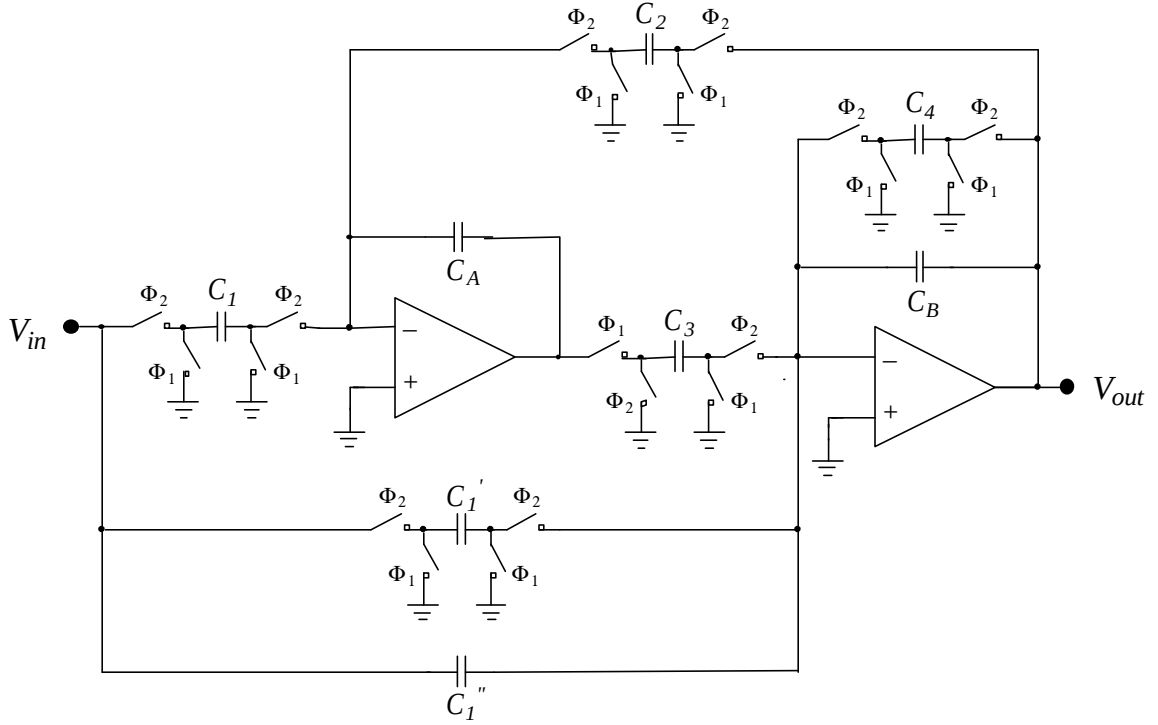


Figure 6-3 S/C-equivalent of the active RC-circuit in Figure 6-2

Replacing all resistors by its equivalent switched capacitors can be done by $|R| = \frac{T}{C}$.

Then the element values of the circuit are determined as:

- $C_1 = \frac{TK_0}{w_0} = |H_{s/c-filter}(0)|w_0T$
- $C_2 = C_3 = w_0T$
- $C_4 = \frac{w_0T}{Q}$
- $C_1' = K_1T$
- $C_1'' = K_2$

(6-5)

FILTERS IMPLEMENTED ON THE FPA

Note that $C_A = C_B = 1u$ because all capacitances are multiple of the unit capacitance u . The symbols Φ_1 and Φ_2 specify the clock phases as described in chapter 2.

The transfer function of this circuit is expressed as:

$$H_{s/c-filter}(s) = \frac{C_1''s^2 + C_1' \frac{1}{T}s + \frac{C_1C_3}{C_A} \frac{1}{T^2}}{C_Bs^2 + C_4 \frac{1}{T}s + \frac{C_2C_3}{C_A} \frac{1}{T^2}} \quad (6-6)$$

The pole frequency ω_0 , which is usually equal to the cut-off frequency of the filter, is much smaller than the clock frequency ω_c , such that the product $\omega_0 T = 2p \frac{\omega_0}{\omega_c}$ is much smaller than 1. In common filter applications, the DC gain of the filter, $|H_{s/c-filter}(0)|$ is bigger than or equal to one and the quality factor Q is less or equal to one, what leads to $\omega_0 T \leq C_1, C_4 < 1$ using equations (6-5). Therefore the ratio of the largest to the smallest capacitor of the circuit, called capacitance spread, is defined by:

$$\frac{C_{\max}}{C_{\min}} = \frac{C_A}{C_2} = \frac{1}{\omega_0 T} \quad (6-7)$$

In general, it is desirable to keep the capacitance spread as small as possible [Gregorian 1986].

All these considerations are based on the assumption that for all used signal frequencies, the clock frequency is many orders higher than the highest signal frequency component. This assumption is usually implied in sampled-data systems. Under this condition the signal voltages are nearly smooth continuous waveforms. However, under these conditions the capacitance spread is very large, as indicated by equation (6-7).

FILTERS IMPLEMENTED ON THE FPAA

As discussed in chapter 2.4, this circuit can be simplified using switch sharing technique. The result is shown in Figure 6-4.

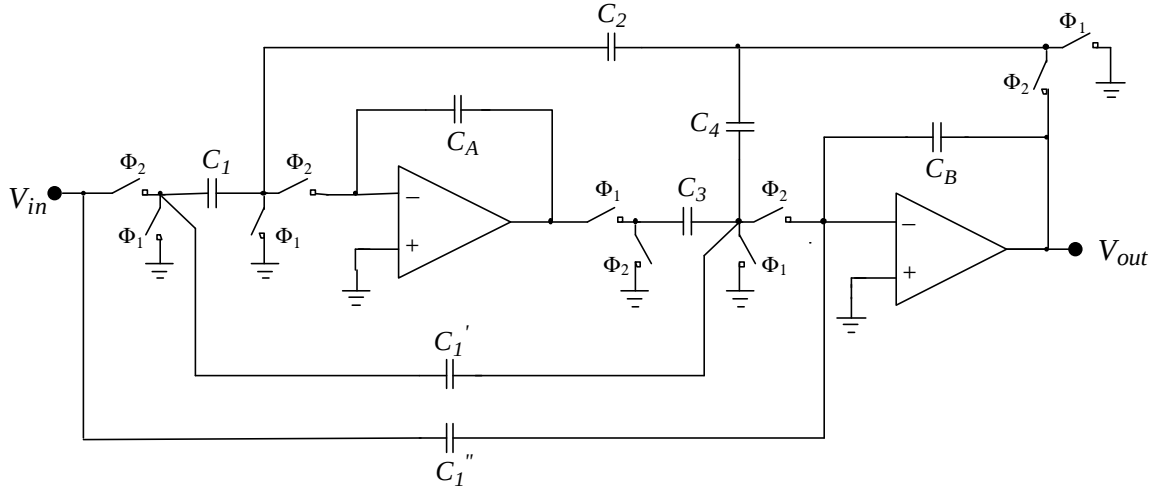


Figure 6-4 S/C filter with switch sharing

The characteristic values such as the corner frequency ω_0 and the quality factor Q can be determined by choosing the appropriate ratio of capacitors. This method can now be applied to all kinds of filters and be implemented on the FPAA.

The theoretical background presented in this chapter is based mainly on [Gregorian 1986] and [Birk 1998].

6.2 Low pass biquad

This macro that can be found in the library of the software EasyAnalog™ is a full cycle low pass filter based on the following biquadratic transfer function:

$$H_{low\ pass}(s) = -\frac{G\omega_0^2}{s^2 + \frac{\omega_0}{Q}s + \omega_0^2}, \quad (6-8)$$

where G is the pass band gain, ω_0 is the corner frequency, and Q the quality factor [MOTOROLA 1997]. There are two different implementations on the FPAA, one for low Q applications ($0.5 < Q < 1$) and additionally one for high Q ($1 < Q < 20$). The circuit designed for low quality factors is illustrated in Figure 6-5.

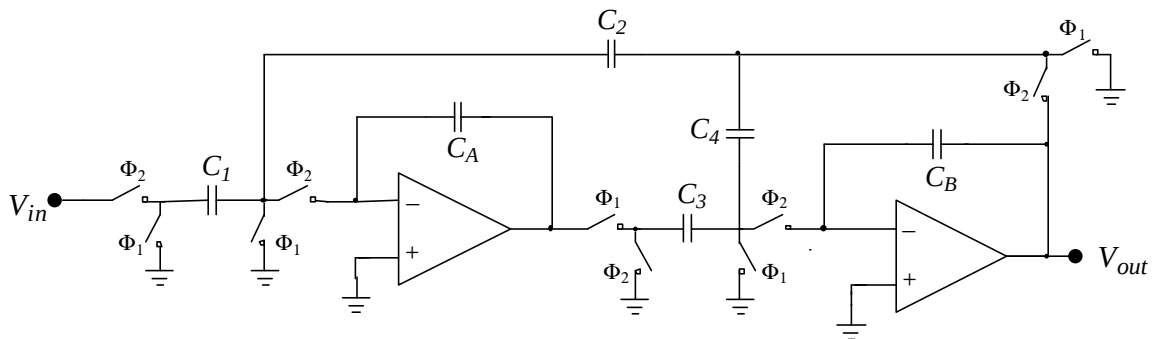


Figure 6-5 Low pass (low Q) filter implementation

FILTERS IMPLEMENTED ON THE FPA

The capacitor values are chosen on the best ratio of capacitors satisfying the desired characteristic values of this filter:[MOTOROLA 1997]

- $w_0 = \frac{C_2}{C_A T} = \frac{C_3}{C_B T}$
- $G = \frac{C_1}{C_2}$
- $Q = \frac{C_3}{C_4}$ (6-9)

The equivalent circuit for high- Q applications is shown in Figure 6-6.

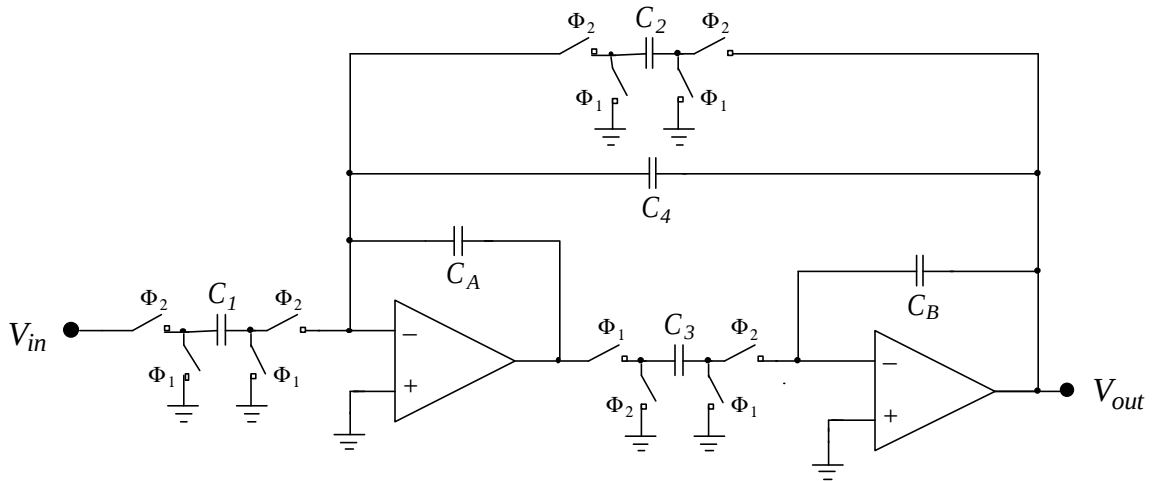


Figure 6-6 Low pass (high- Q) filter implementation

For every filter of 2nd order two implementations for the different Q ranges, such as low- Q ($0.5 < Q < 1$) and high- Q ($1 < Q < 20$), exist. The investigations in this thesis are mainly concentrated on high- Q biquads. Therefore, the following filters are presented only for high- Q implementations. Analogous techniques can be used for low- Q biquads.

6.3 High pass biquad (high-Q)

The transfer function of the high pass biquad (high-Q) is:

$$H_{high\,pass}(s) = -\frac{G s^2}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}, \quad (6-10)$$

with G as pass band gain, ω_0 as the corner frequency, and Q as the quality factor as mentioned before in chapter 6.2. The implemented macro realizing this transfer function is shown in Figure 6-7.

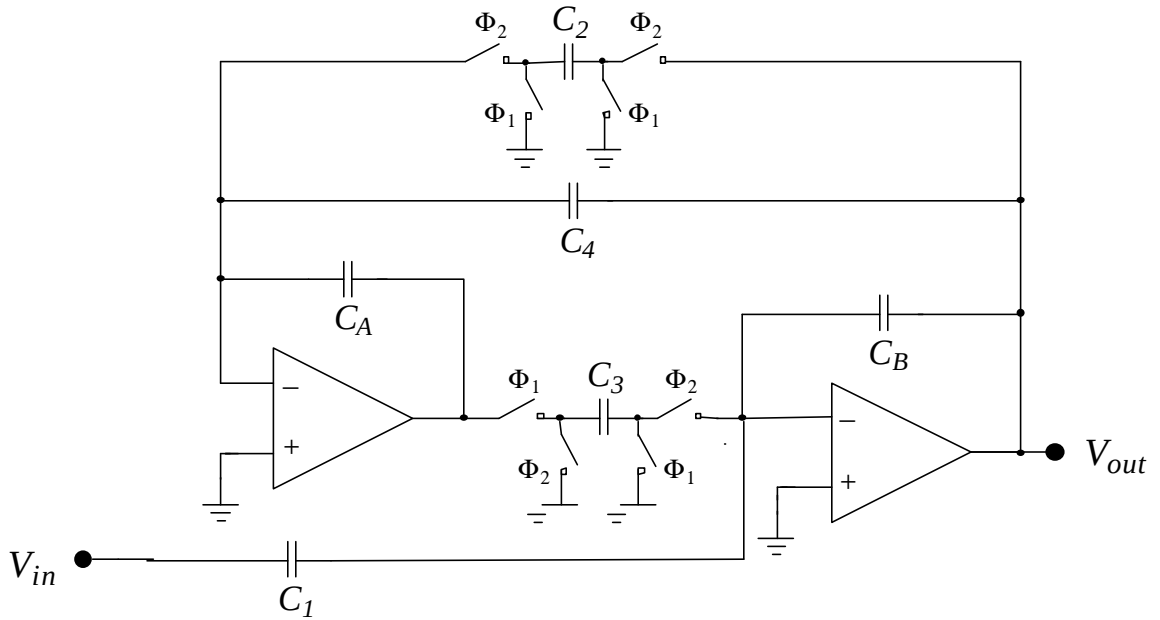


Figure 6-7 High pass (high-Q) filter implementation

FILTERS IMPLEMENTED ON THE FPAA

The characteristic values of the filter can be determined by [MOTOROLA 1997]:

- $w_0 = \frac{C_2}{C_A T} = \frac{C_3}{C_B T}$
- $G = \frac{C_1}{C_B}$
- $Q = \frac{C_A}{C_4}$ (6-11)

These relations are used to determine the filter parameters in the experimental investigations and model validation studies.

6.4 Band pass biquad (high-Q)

The transfer function of the band pass (high-Q) biquad is

$$H(s) = - \frac{G \frac{w_0}{Q} s}{s^2 + \frac{w_0}{Q} s + w_0^2}, \quad (6-12)$$

where, as before, G is pass band gain, Q the quality factor, but ω_0 is the center frequency of the filter spectrum. The circuit that realizes the macro is illustrated in Figure 6-8.

FILTERS IMPLEMENTED ON THE FPAA

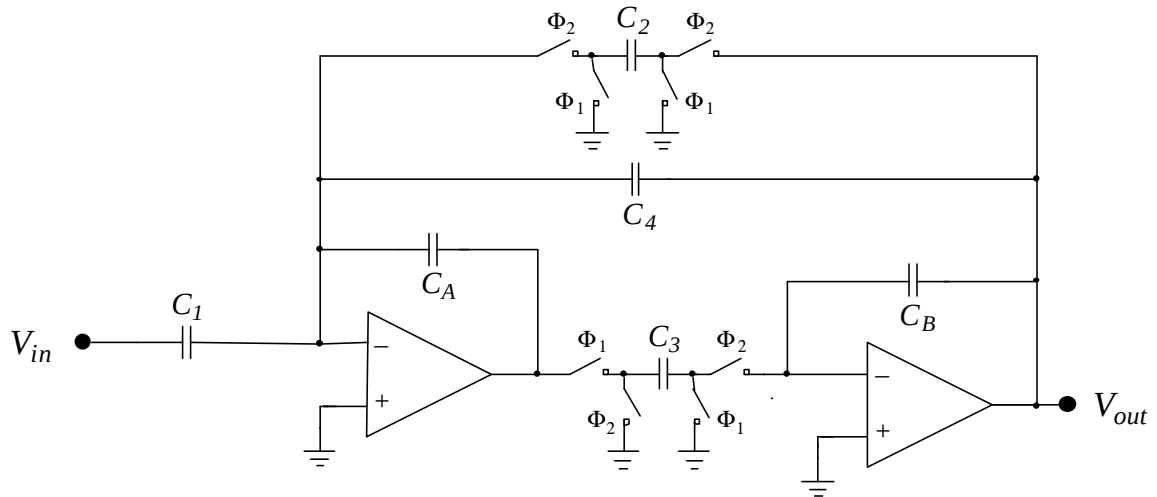


Figure 6-8 Band pass (high-Q) filter implementation

To determine the desired filter parameter values the capacitors have to satisfy the following relationships: [MOTOROLA 1997]

- $\omega_0 = \frac{C_2}{C_A T} = \frac{C_3}{C_B T}$
- $G = \frac{C_1}{C_4}$
- $Q = \frac{C_A}{C_4}$ (6-13)

FILTERS IMPLEMENTED ON THE FPAA

A bandwidth with 3dB-attenuation is defined by the ratio of the corner frequency to the quality factor, thus:

$$\bullet \quad 3dB - bandwidth = \frac{\omega_0}{Q} = \frac{C_4}{C_B T} = \frac{C_2 C_4}{C_A C_3 T} \quad (6-14)$$

The *3dB-bandwidth* describes the range of the pass-band of the filter, where the signal is not blocked until it reaches an attenuation of 3-dB at the borders of the pass-band.

6.5 Band stop biquad (high-Q)

The transfer function of a general band stop biquad is given by

$$H_{band\ stop}(s) = -\frac{G_H s^2 + \omega_0^2 G_L}{s^2 + \frac{\omega_0}{Q} s + \omega_0^2}, \quad (6-15)$$

where Q is the quality factor, ω_0 the center frequency of the stop band, G_H the high frequency pass band gain, and G_L the low frequency pass band gain. The circuit that realizes this transfer function on the FPAA is shown in Figure 6-9.

FILTERS IMPLEMENTED ON THE FPAA

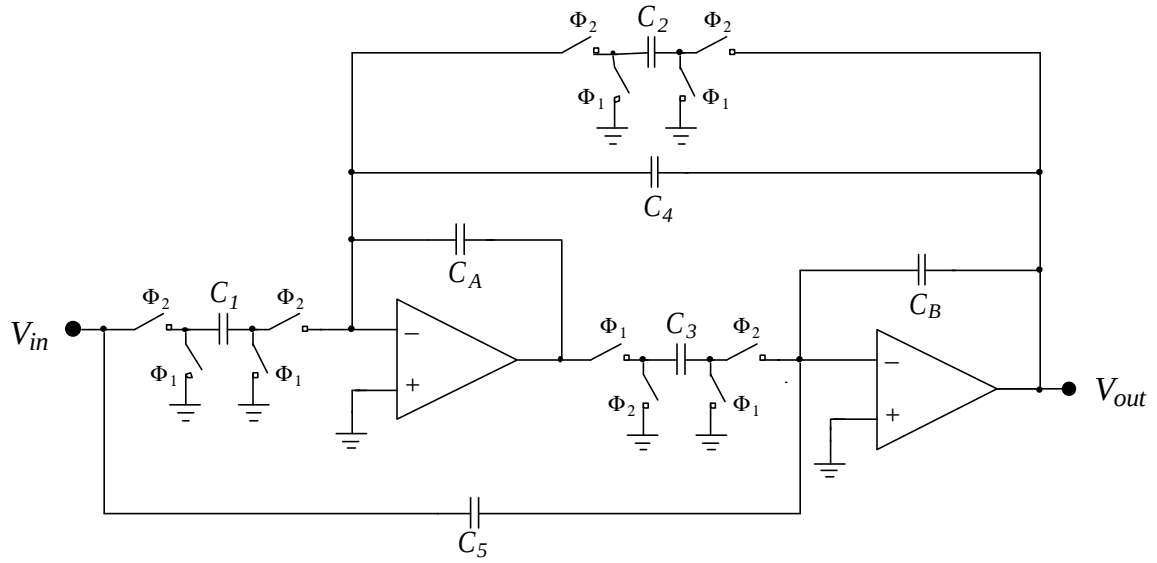


Figure 6-9 Band stop (high-Q) filter implementation

The characteristic values of the filter can be determined by: [MOTOROLA 1997]

- $w_0 = \frac{C_2}{C_A T} = \frac{C_3}{C_B T}$
 - $G_L = \frac{C_1}{C_2}$
 - $G_H = \frac{C_5}{C_B}$
 - $Q = \frac{C_A}{C_4}$
- (6-16)**

FILTERS IMPLEMENTED ON THE FPAA

and a notch frequency can be derived at:

$$\text{Notch frequency} = \omega_0 \sqrt{\frac{G_L}{G_H}} = \omega_0 \sqrt{\frac{C_1 C_B}{C_2 C_5}} . \quad (6-17)$$

The *notch frequency* is the frequency component that is blocked by a band stop filter with a very narrow stop-band.

These filters are included in the library of the software EasyAnalog™ and therefore the chip can be programmed easily using these macros and changing their characteristic values.

7. TIME BEHAVIOR OF SYSTEM FUNCTIONS

7.1 Time response analysis

In order to investigate the transition behavior of an implemented analog function from the programming phase, when the entire circuit is at zero initial conditions, until the steady-state status of the analog function, it is necessary to perform a dynamic response analysis of a transfer function that can be described by a ratio of two polynomials. The response depends upon the characteristic parameters of the system function and the input of the system.

As already mentioned in chapter 3.4 the FPAA works with a signal ground of 2.5V that is reached right after the programming phase, where the entire chip is set to earth ground. Considering this ‘jump’ of 2.5V from earth to signal ground, we assume that the input is a step function of high amplitude overlaid with a sinusoidal signal with much smaller amplitude. Thus, it is necessary to investigate the step response of the system function.

The following analysis is not restricted to the indicated example but is valid for a general second-order type-1 system, which is characterized by two poles and no zeros. The standard form of a second order system with no zeros is defined as

$$H(s) = \frac{\omega_n^2}{s^2 + 2\zeta\omega_n s + \omega_n^2} = \frac{p(s)}{q(s)}, \quad (7-1)$$

where ζ is the *damping factor* of the system and ω_n is the *undamped natural frequency* in rad/s. The time response of any system is characterized by the roots of the denominator polynomial $q(s)$, which describes the poles of the system transfer function and is called the *characteristic polynomial*.

To determine the poles of the system one has to set

TIME BEHAVIOR OF SYSTEM FUNCTIONS

$$q(s) = 0. \quad (7-2)$$

Equation (7-2) is called the *characteristic equation* of the transfer function. The solution of the characteristic equation can be used to write:

$$s^2 + 2zw_n s + w_n^2 = (s - s_1)(s - s_2) = 0. \quad (7-3)$$

For $z < 1$ the poles are

$$s_1, s_2 = -zw_n \pm jw_n \sqrt{1 - z^2} = -zw_n \pm jw_d, \quad (7-4)$$

where $w_d = w_n \sqrt{1 - z^2}$ is called the *damped natural frequency*. Usually the parameters of a second-order system are chosen such that the damping factor is smaller than one: $z < 1$. Therefore only this case will be investigated more closely in this section. Applying equation(7-4) on (7-1) and using the unit-step function as input leads to

$$Y_{Step}(s) = \frac{w_n^2}{s(s + zw_n - jw_n \sqrt{1 - z^2})(s + zw_n + jw_n \sqrt{1 - z^2})} \quad (7-5)$$

The inverse Laplace transformation gives the time response of the system in the form [Nagrath 1975]:

$$\begin{aligned} y_{Step}(t) &= \left. \frac{w_n^2}{s^2 + 2zw_n s + w_n^2} \right|_{s=0} + 2\Re \left\{ \left. \frac{w_n^2}{s(s + zw_n - jw_n \sqrt{1 - z^2})} \right|_{s = -zw_n - jw_n \sqrt{1 - z^2}} \right\} \\ &= 1 - \frac{e^{-zw_n t}}{\sqrt{1 - z^2}} \sin \left[w_n \sqrt{1 - z^2} t + \tan^{-1} \frac{\sqrt{1 - z^2}}{z} \right] \end{aligned} \quad (7-6)$$

The steady-state value of this function after the settling process is given by:

TIME BEHAVIOR OF SYSTEM FUNCTIONS

$$y_{ss} = \lim_{t \rightarrow \infty} y_{Step}(t) = 1 \quad (7-7)$$

This value will be reached after the settling time because of the decaying exponential function that is characterized by the damping factor ζ . Thus the steady-state error is zero. The signal shape is a damped sinusoidal that oscillates between a pair of decaying exponential envelopes before it reaches the final value y_{ss} as illustrated in Figure 7-1:

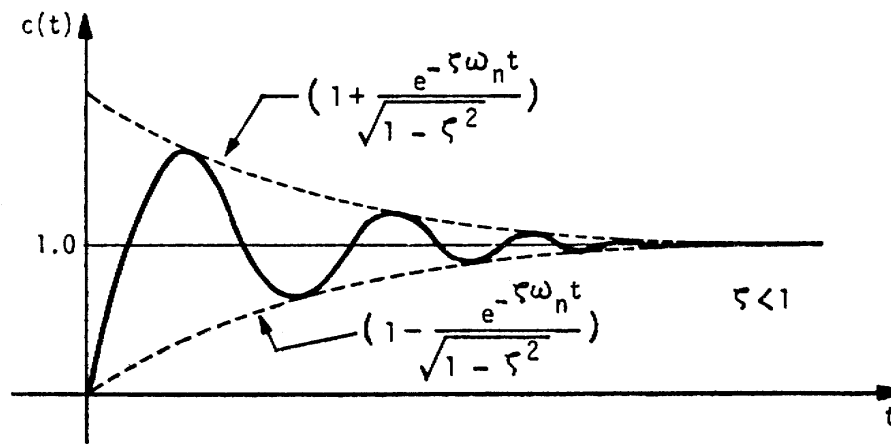


Figure 7-1 Unit-step response of a underdamped ($\zeta < 1$) second-order system

7.2 The damping factor ζ

As ζ increases, the response becomes progressively less oscillatory till it reaches a non-oscillatory shape for $\zeta=1$, above which the signal never goes above the steady-state value y_{ss} . When $\zeta > 1$ the system is called overdamped. On the other hand the system breaks

TIME BEHAVIOR OF SYSTEM FUNCTIONS

into continuous oscillation without losing magnitude for $\zeta=0$. The step response for various ζ is shown in Figure 7-2:

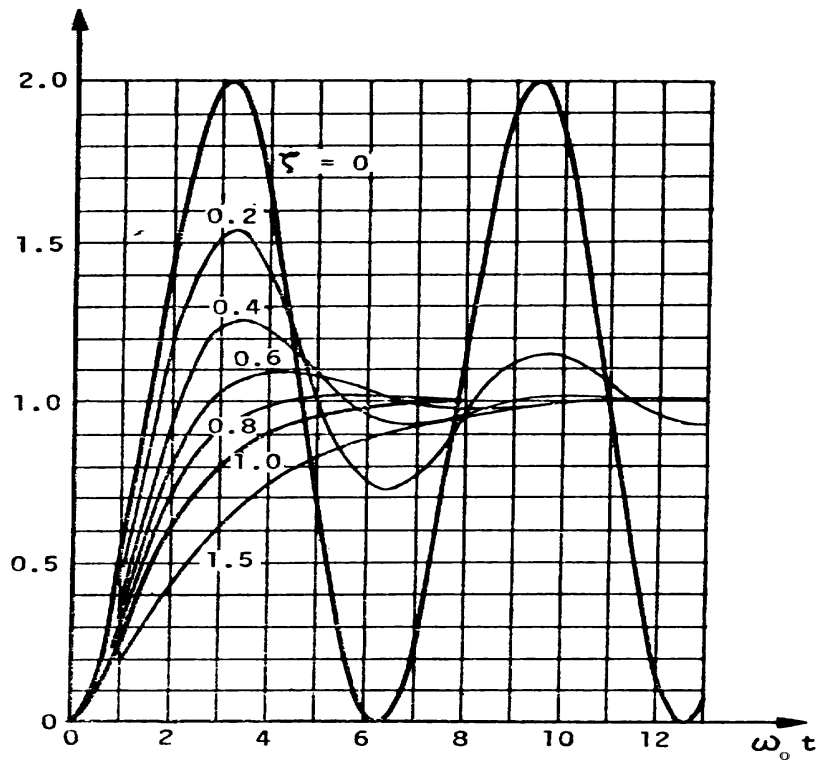


Figure 7-2 Step response curves of second-order systems for different ζ

This graph shows how the damping factor determines the decay of the oscillating signal. The main question of this analysis is now, how long it takes to practically reach the final steady-state value y_{ss} for different characteristic parameters such as the damping factor ζ and the undamped natural frequency ω_n . This time period is called *settling time* and can be determined using the time response on the unit-step input (7-6).

7.3 The settling time t_s

It is obvious that the signal never crosses the exponential ‘boundaries’ of the oscillating term. Applying a tolerance band of 1% onto the steady-state value y_{ss} the exponential term of the step response (7-6) reaches this band after the settling time t_s and stays within that band. It can be observed that as the damping factor ζ is reduced from the value of one, corresponding to the critical damping case, the normalized settling time $\omega_n t_s$ decreases monotonically until the first overshoot just stays below the upper tolerance boundary. If the damping is decreased further, the normalized settling time suddenly increases nonlinearly. This happens because the maximum of the first overshoot is higher than the upper boundary of the steady-state value, and the settled state is reached after the backslide of the first overshoot. Thus, the normalized settling time has a discontinuity, and then increases slightly with further decrease in damping. It is the smallest at the first discontinuities, therefore transfer functions of second-order, as in control theory, are normally designed to be underdamped to provide short settling behavior. For relatively small values of damping, the time response oscillates significantly between the exponential ‘envelopes’ and an approximate expression for the settling time can be easily obtained by finding the time when the exponential envelopes stay within this tolerance band. The settling time can be then determined, using (7-6), as:

$$\frac{e^{-\zeta \omega_n t_s}}{\sqrt{1 - \zeta^2}} = 0.01 \quad (7-8)$$

For very low values of the damping factor ζ we can assume that the value of the square root is one and we achieve:

$$e^{-\zeta \omega_n t_s} \approx 0.01. \quad (7-9)$$

The settling time for second-order systems (low values of ζ) is thus defined as:

TIME BEHAVIOR OF SYSTEM FUNCTIONS

$$t_s = \frac{4.605}{zw_n}. \quad (7-10)$$

Additional approximation with a 2% tolerance band for the settling time is given by $t_s = 4T$, where T is the time constant of the exponential term that limits the oscillating term of the step response.

This analysis holds exactly for a second-order type-1 transfer function with no zeros and is mainly based on [Nagrath 1975], [Truxal 1958] and [Goeldner 1970].

7.4 Systems of second order with zeros

Let us now consider the effect of a zero in the transfer function on system performance. The transfer function of a second-order system with one zero at $s = -z$ is given by:

$$\begin{aligned} H_{zero}(s) &= \frac{Y(s)}{X(s)} = \frac{(s+z)\frac{w_n^2}{z}}{s^2 + 2zw_n s + w_n^2} \\ &= \frac{w_n^2}{s^2 + 2zw_n s + w_n^2} + \frac{s}{z} \left[\frac{w_n^2}{s^2 + 2zw_n s + w_n^2} \right]. \end{aligned} \quad (7-11)$$

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The time response of the system on a step input, using (7-11), is then:

$$y_z(t) = y(t) + \frac{1}{z} \frac{d}{dt} c_y b_t q h, \quad (7-12)$$

where $y(t)$ is the response of the appropriate system without zero.

The effect of an additional zero on the step response is shown in Figure 7-3 [Nagrath 1975]:

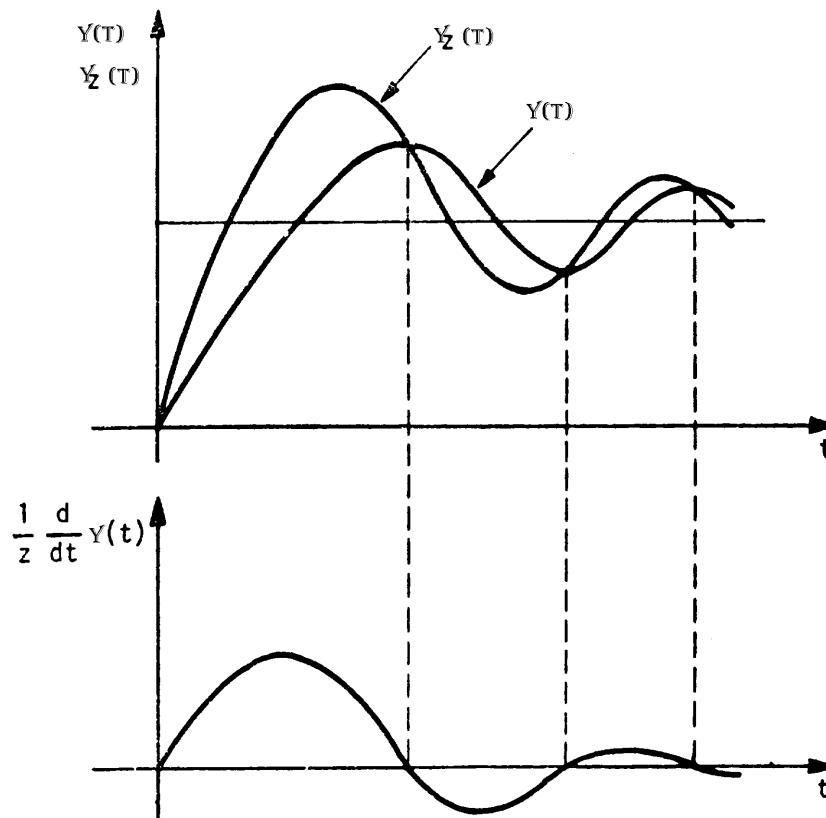


Figure 7-3 Effect of an additional zero on unit-step response of 2nd-order systems

TIME BEHAVIOR OF SYSTEM FUNCTIONS

Figure 7-3 shows that the additional zero in the transfer function adds a pronounced early peak to the system response without a zero. The overshoot increases significantly. It can be shown that the smaller the value of z , the more pronounced is the additional peaking effect. Therefore it is desirable to avoid zeros close to the real axis in system design. This effect cannot influence the settling time significantly because the additional part caused by the zero is also decaying with the exponential envelope as illustrated in the lower diagram of Figure 7-3 and is therefore almost zero at the time when the original signal has entered the tolerance boundaries.

7.5 Settling time of the biquads of the FPAA

Let us use now the analysis presented in chapter 7.3 for the filter functions that can be chosen from the library of EasyAnalog™ in order to implement them into the FPAA. Inspection of the transfer functions of the different biquad filters establishes a general transfer function without zeros, in fact identical to the transfer function of a low pass filter, as:

$$H_{biquad}(s) = -G \frac{4p^2 f_0^2}{s^2 + \frac{2pf_0}{Q}s + 4p^2 f_0^2}, \quad (7-13)$$

where G is the pass-band gain, f_0 is the corner frequency in Hz , and Q the quality factor of the filter.

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Comparing (7-13) with (7-1) the following relationships are obtained:

$$f_0 \equiv \frac{w_n}{2p} \equiv \frac{w_0}{2p} \quad (7-14)$$

and
$$Q \equiv \frac{1}{2z} \quad (7-15)$$

The relationship of (7-15) shows that the quality factor is not only characterizing the transient from the pass-band to the stop-band in the frequency response but also the oscillation of the settling behavior. With the restriction of $\zeta < 1$ we obtain a requirement for the quality factor of the filters: $Q > 0.5$.

Applying the relationships of (7-14) and (7-15) to the equation for the settling time of a general second-order transfer function (7-10) leads to the settling time of biquad filters as:

$$t_{biquad} = \frac{4.605Q}{pf_0} \quad (7-16)$$

This equation shows the dependencies of the settling time of the biquads on the filter characteristics, such as the corner frequency and the quality factor. Values for the settling time for filters with various values of Q and ω_0 , which can be achieved by the technology of the FPAA, are shown in the following graphs. To get a better graphical illustration of the shape of the settling time two graphs are shown.

TIME BEHAVIOR OF SYSTEM FUNCTIONS

The lower frequency range, from 8 to 50kHz, is illustrated in Figure 7-4:

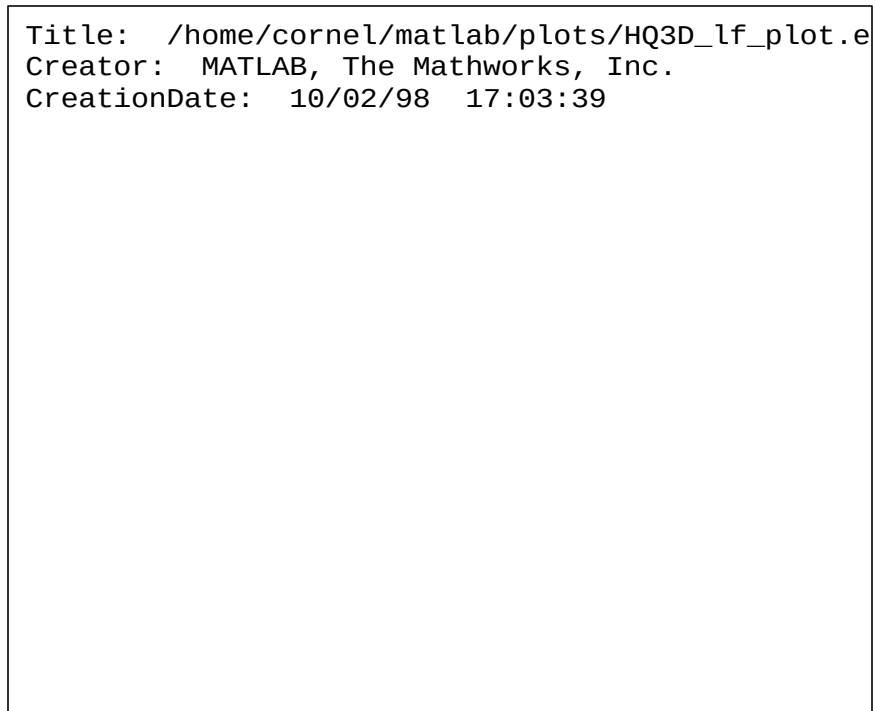
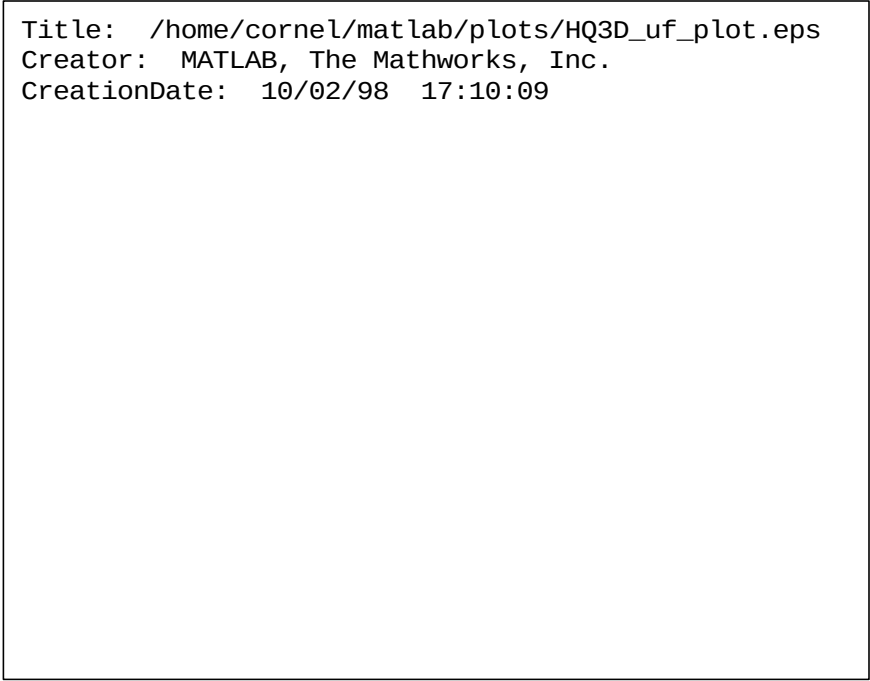


Figure 7-4 Settling time of 2nd-order systems in lower frequency range.

The settling time of values in the upper frequency range, from 50 to 100kHz, is much smaller, therefore it is represented on a separate plot in Figure 7-5 with a different scale on the time axis.

TIME BEHAVIOR OF SYSTEM FUNCTIONS



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Figure 7-5 Settling time of 2nd-order systems in higher frequency range

These graphs indicate that the settling time increases significantly with increasing quality factor, especially for very low corner frequencies. Therefore, the time delay for the switching of the output of the reconfigured FPAA has to be adjusted appropriately in order to avoid perturbations. This time delay must be particularly long for the filters implemented with a low corner frequency and a high quality factor.

8. MEASUREMENTS OF SETTLING TIME OF 2ND-ORDER FILTERS

8.1 *Step function as input signal*

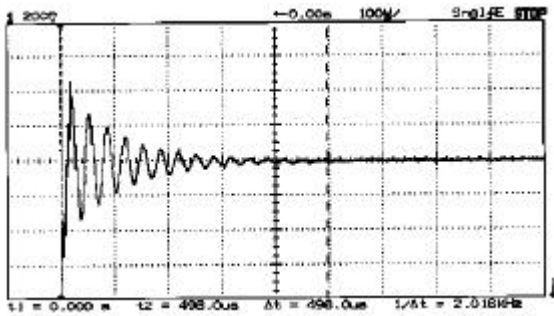
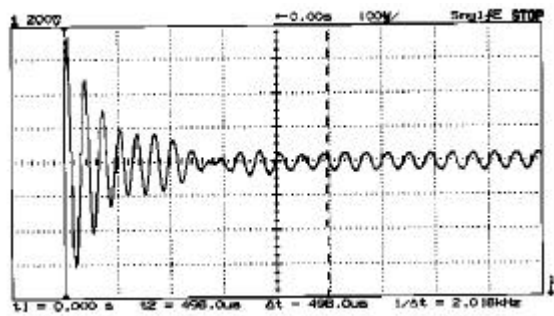
The measurements were performed to verify the theoretical results of chapter 7.5 using the second-order filter implementations given by the software EasyAnalog™.

The first measurements made clear that it is difficult to determine exactly the settling time for sinusoidal signals typically used in filter applications. The theoretical investigations of chapter 7.1 predicted that the output signal is oscillating between a pair of exponential decaying envelopes before reaching the steady-state. Considering that the sinusoidal input signal is superimposed on the signal ground of 2.5V, we assume that the sinusoidal signal is also overlaid on the exponential shape of the step response as already discussed in chapter 5.1. Various measurements showed that the settling time of sinusoidal input signals is equal to the settling time of a constant step input, as shown in Figure 8-1. Identical filter were used for both graphs, with a sinusoidal input signal on top, and a constant input on the bottom. The two columns show 2 filters, a band pass biquad with corner frequency of $f_0 = \frac{\omega_0}{2\pi} = 30kHz$ and a quality factor of $Q = 10$, and a high pass

biquad with a corner frequency of $f_0 = \frac{\omega_0}{2\pi} = 20kHz$, and a quality factor of $Q = 10$.

MEASUREMENTS OF SETTLING TIME OF 2ND-ORDER FILTERS

Band pass biquad



High pass biquad

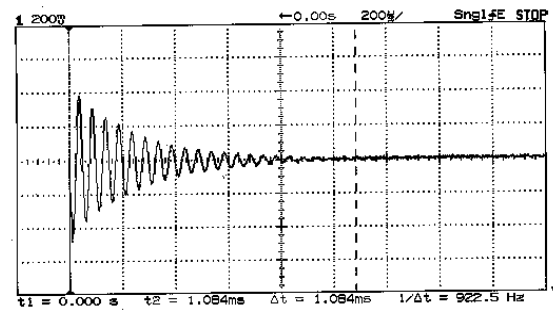
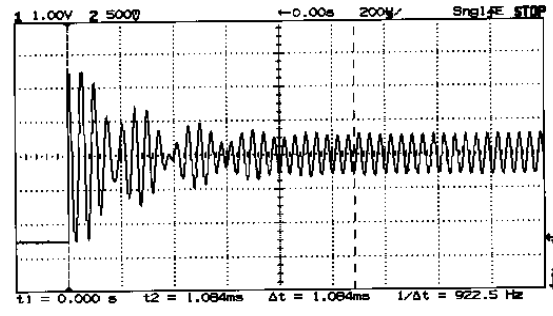


Figure 8-1 Comparison of measured filter response to sinusoidal (top) and constant (bottom) input signals

For both, the sinusoidal signal and the constant signal, the typical exponential envelopes were observed and are disappearing at the same time which is represented in Figure 8-1 by the dotted line. From this dotted line on both signals show the desired constant behavior at the output.

All the following measurements were performed using constant input signals in order to get a better determination of the settling time by the oscilloscope.

8.2 Aspects of measurements

As already presented in chapter 7.5, the settling time is a linear function of the quality factor Q and the reciprocal value of the corner frequency ω_0 . Measurements were done for varying quality factors for the four different filters to determine the settling time via the oscilloscope. The measurements were performed to verify the theoretical results of chapter 7 using the second-order filter implementations given by the software EasyAnalog™. A constant pass band gain of $G=1$ was used in all measurements. The low resolution of the oscilloscope made it difficult to get the exact time when the signal deviation is smaller than 1%. Especially for low settling time values in the high frequency range and for quality factors smaller than a value of one it is very difficult to obtain meaningful measured results, therefore there are only results of measurements with high- Q ($1 < Q < 20$) filters presented. Additionally, the measured points were not situated exactly on a ‘straight line’. In order to get a more meaningful analysis of the measured values, the measurements were linearized into a straight line by the method of linear regression [Weisberg 1985].

8.3 Linear regression

The method of linear regression is commonly used to study relationships between measurable variables that can be described by straight lines, or by generalizations of straight lines to many dimensions. These techniques are applied in almost every field of study, including social sciences, physical and biological sciences, business and technology, and the humanities. The most common reason for linear regression models is a

MEASUREMENTS OF SETTLING TIME OF 2ND-ORDER FILTERS

description of a relationship of measured data and a prediction for future values. Generally, regression analysis consists of many steps. To study a relationship between a number of variables, data is collected on each of a unit or case of these variables. In the regression model used in this work, one measured point corresponds to one appropriate unit. The hypothesized model specifies the behavior of the response for given values of the predictors and some of the characteristics of the failure to provide an exact fit through hypothesized error terms. Then, the data is used to obtain estimates of the unknown parameters. The method of estimation used for this linearization is least squares, although there in fact exist various estimation procedures. In simple regression, the relationship between two one-dimensional variables, say X and Y , is studied. Assuming that the relationship can be described by a straight line, one can apply the model of linear regression. The equation of a straight line relating two quantities X and Y can be defined as:

$$Y = mX + Y_0 \quad (8-1)$$

In equation (8-1), m is the slope of the straight line, defined as the rate of change in Y for a unit change of X , and Y_0 as the intercept, the value of Y when X is zero. Y_0 and m are parameters and can present all possible straight lines by ranging over all possible values. However, in reality measured data will almost never fall exactly on a straight line. The differences between the measured values and the values given by the model, usually called statistical errors, account for the failure of the model to provide an exact fit. The most important error source for these differences are measurement inaccuracies, such as reading errors or influence of the measurement devices. Let e_i , $i=1,2,\dots,n$, be the value of the statistical error for the i th case:

$$e_i = y_i - (Y_0 + mx_i), \quad i = 1, 2, \dots, n \quad (8-2)$$

It is assumed that the errors are all of random nature and fixed components are negligible, the e_i have a zero mean $E(e_i)=0$, $i=1,2,\dots,n$. An additional convenient

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assumption is that the errors e_i are uncorrelated and have a common variance $\text{var}(e_i) = \sigma^2$, $i=1,2,\dots,n$. Heuristically, uncorrelated means that the value of one error does not depend on or influence the value of another one.

We have set now X and Y to be the predictor and the response, respectively, with measured values (x_i, y_i) of X and Y for $i=1,2,\dots,n$. We define e_i as the statistical error of (x_i, y_i) . The linear regression model specifies the following:

$$y_i = Y_0 + mx_i + e_i \quad i = 1, 2, \dots, n \quad (8-3)$$

$$\text{with } E(e_i) = 0, \quad \text{var}(e_i) = \sigma^2, \quad \text{cov}(e_i, e_j) = 0, \quad i \neq j$$

In words, the model says that the observed value y_i can be determined from the value of x_i through the specified equation of (8-3), except that the statistical error e_i , an unknown value, is added on. The three quantities m , Y_0 , and σ^2 are also unknown. The single errors e_i are unobservable quantities introduced into the model to account for the failure of the measured data with respect to the linear fit. Only the x_i - and y_i -parameters are observed values and this data is used to obtain estimates for the unknown parameters as m , Y_0 , and σ^2 , and thus the desired system relationship. The method of error minimization is called least squares, in which parameters are chosen to minimize a quantity called the residual sum of squares. The unknown parameters, that are being estimated statistically in the model in order to minimize the statistical error, are denoted with a little “hat” over the corresponding letter, for example $\hat{m}$ is the estimated value for the slope m . Using this notation we can identify the fitted values determined by the estimated regression equation as:

$$\hat{y}_i = \hat{Y}_0 + \hat{m}x_i, \quad i = 1, 2, \dots, n, \quad (8-4)$$

where $\hat{y}_i$, $\hat{Y}_0$, and $\hat{m}$ are the estimated parameters in contrast to the observed parameter x_i .

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Thus the observed fitting errors or residuals, denoted by $\hat{e}_i$, are given by:

$$\hat{e}_i = y_i - (\hat{Y}_0 + \hat{m}x_i), \quad i = 1, 2, \dots, n, \quad (8-5)$$

which should be compared to the equation for the statistical errors (8-2). The difference between e_i and $\hat{e}_i$ is important, as the residuals are observable and will be used to verify the assumptions, while the statistical errors are not observable. Comparing (8-5) to (8-4) leads to:

$$\hat{e}_i = y_i - \hat{y}_i, \quad i = 1, 2, \dots, n \quad (8-6)$$

This is the basic criterion function for obtaining estimators by the method of least squares. The residuals e_i give the vertical distances between the measured value y_i and the estimated value $\hat{y}_i$. There are other criteria for choosing an estimator, but the residuals are a good choice because they reflect the inherent asymmetry in the roles of the response and the predictor in regression problems. The least square estimators are the values $\hat{Y}_0$ and $\hat{m}$ that minimize the expression

$$RSS(\hat{Y}_0, \hat{m}) = \sum_{i=1}^n [y_i - (\hat{Y}_0 + \hat{m}x_i)]^2. \quad (8-7)$$

$RSS(\hat{Y}_0, \hat{m})$ is called the *residual sum of squares*, or just *RSS*. A method of minimizing (8-7) is to differentiate with respect to $\hat{Y}_0$ and $\hat{m}$, set the derivatives equal to zero to find the minimum, and solve the resulting equations. Carrying out this plan yields

$$\frac{\partial RSS(\hat{Y}_0, \hat{m})}{\partial \hat{Y}_0} = -2 \sum_{i=1}^n (y_i - \hat{Y}_0 - \hat{m}x_i) \equiv 0 \quad (8-8)$$

$$\text{and} \quad \frac{\partial RSS(\hat{Y}_0, \hat{m})}{\partial \hat{m}} = -2 \sum_{i=1}^n x_i (y_i - \hat{Y}_0 - \hat{m}x_i) \equiv 0. \quad (8-9)$$

Rearranging (8-8) and (8-9) becomes

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$$\hat{Y}_0 n + \hat{m} \sum_{i=1}^n x_i = \sum_{i=1}^n y_i \quad (8-10)$$

$$\text{and} \quad \hat{Y}_0 \sum_{i=1}^n x_i + \hat{m} \sum_{i=1}^n x_i^2 = \sum_{i=1}^n x_i y_i \quad (8-11)$$

These equations are called the *normal equations* for model (8-3). Combining and rearranging (8-11) leads to the desired equation for the estimated slope:

$$\hat{m} = \frac{\sum_{i=1}^n x_i y_i - \frac{1}{n} \sum_{i=1}^n x_i \sum_{i=1}^n y_i}{\sum_{i=1}^n x_i^2 - \frac{1}{n} (\sum_{i=1}^n x_i)^2} = \frac{SXY}{SXX}, \quad (8-12)$$

where SXY is defined as the corrected sum of cross products of x_i and y_i and SXX as the corrected sum of squares of x_i . The second estimate parameter $\hat{Y}_0$ is given by

$$\hat{Y}_0 = \frac{1}{n} \sum_{i=1}^n y_i - \hat{m} \frac{1}{n} \sum_{i=1}^n x_i = \bar{y} - \hat{m} \bar{x}, \quad (8-13)$$

where $\bar{y}$ and $\bar{x}$ are the sample average for the measured data x_i and y_i . Applying these two estimated parameters to the estimated regression equation (8-4) creates the desired fitting straight line for the measured data. Using this fit and neglecting the statistical errors of the diverse measurements allows a more meaningful analysis of the measured data.

By dividing the residual sum of squares RSS by $(n-2)$, we obtain a measure known as the residual variance [Edwards 1976]:

$$s_{Y.X}^2 = \frac{\sum_{i=1}^n (y_i - \hat{y}_i)^2}{n-2} = \frac{RSS(\hat{Y}_0, \hat{m})}{n-2}. \quad (8-14)$$

The residual variance $s_{Y.X}^2$ is a measure of the variation of the y_i values around the regression line. The dot separating the Y and X subscripts indicates that the regression line

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is that of Y on X , that we are predicting Y values from the corresponding X values. The residual variance is in fact an estimate for the ‘usual’ variance σ^2 , that is essentially the average squared size of the statistical errors e_i and is also often named as *residual mean square*. In general, any sum of squares divided by its degree of freedom, here $(n-2)$, is called a mean square. This variable is in the same unit as is the variable Y . If we now take the square root of the residual variance, we obtain the standard error of estimate:

$$s_{Y.X} = \sqrt{s_{Y.X}^2} = \sqrt{\frac{\sum_{i=1}^n (y_i - \hat{y}_i)^2}{n-2}} \quad (8-15)$$

The standard error of estimate $s_{Y.X}$ is also a measure of the variability of the y_i values about the regression line of Y on X and is used in this thesis in order to ascertain a measure for the deviations of the actual measured values to the linearized fit for the different filters.

8.4 A minimum boundary for the settling time

During various measurements it was discovered that for very low quality factors and high corner frequencies, which would allow for a very short settling time, the measured settling time was much higher than expected.

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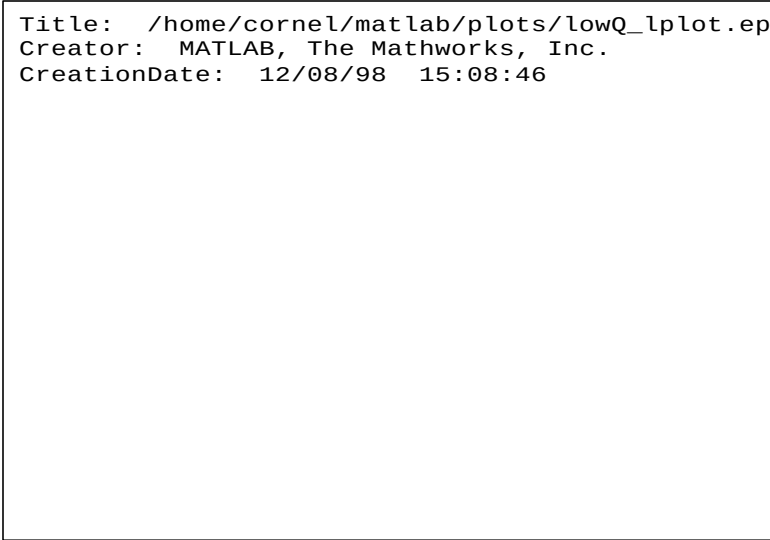


Figure 8-2 **Measurements and the linear fit of a high pass (low- Q) biquad at corner frequency of 25kHz in low- Q range**

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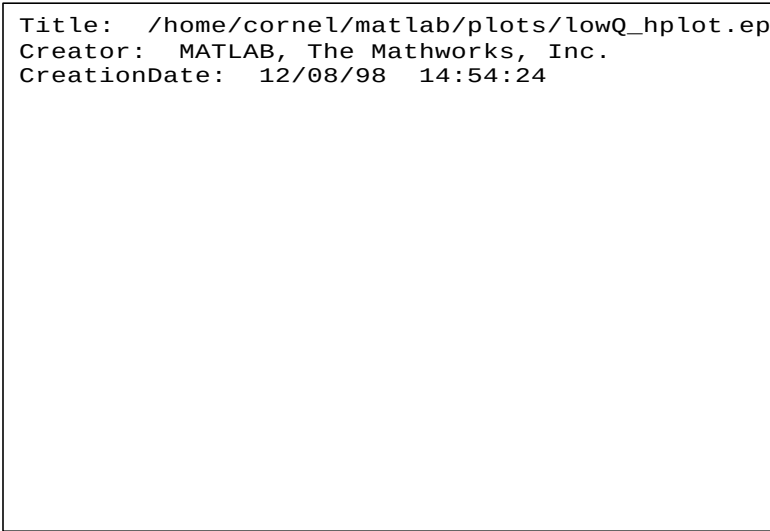


Figure 8-3 **Measurements and linear fit of a high pass (high- Q) biquad at corner frequency of 25kHz in entire Q range including the linear fit (dotted) of Figure 8-2.**

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Figure 8-2 and Figure 8-3 show this effect, where measurements with a high- Q high pass filter and the appropriate low- Q filter were carried out for varying quality factors Q down to the minimum possible quality factor of $Q=0.5$. Figure 8-2 shows the data of a high pass low- Q biquad and its linearized straight (dotted) line. This dotted line does not cross the origin and is included in Figure 8-3, where the measurements and the linearized straight (solid) line of the appropriate filter for the high- Q range are shown additionally. These two lines do not match each other. For values smaller than one of the quality factor the settling time of the low- Q values is much higher than the linearized straight line of the high- Q biquad measurements. Additionally, for values above this critical parameter of $Q=1$ the linear fit of the low- Q data (dotted line) delivers values for the settling time that are less than half of the values of the linear straight derived by the high- Q filter data. This effect, which can be observed on all filter measurements, has two reasons. First, a value for the settling time smaller than the minimum value of approximately $t_{s,min}=50\mu s$ was never reached during any of the measurements. The technology of the FPAA seems to provide a kind of a ‘natural boundary’ for the speed that a signal needs to settle when the chip starts to work. This ‘natural boundary’ for the settling time is also observed and illustrated in chapter 9 with the measurements of systems of higher order. Second, the reading errors are much bigger in the range of very low settling times because it is much more difficult to determine the settling time for a signal that reaches its steady-state value in a very short time. Figure 8-4 shows how difficult it is to get an exact value for the time where the exponential envelope has decayed down to the 1%-boundary of the steady-state value, if the signal barely oscillates within these envelopes, as shown in the left picture.

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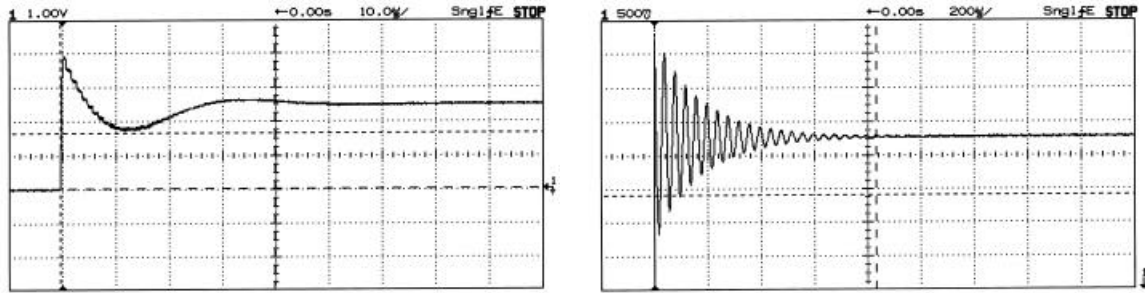


Figure 8-4 Reading uncertainties of settling time

For higher values of the settling time, such as shown one on the right, it is easy to identify the exponential curve because there are so many points of the oscillating term that touch the wrapping boundaries in contrast to the two or three points shown in the left picture. Consequently, the values of the low- Q range are not accurate. That is the reason why the main focus of this study is on measuring high- Q filters during these investigations.

Another aspect of this effect should also be considered. The values in the low- Q range are usually above the linearized straight line of the measurements and create a high offset Y_0 for the equation of the linear regression. Knowing the ‘natural boundary’ for the settling time and the percentual higher reading errors in that range, the influence of this effect should be minimized during the linearization. An easy method to perform this is to neglect the offset Y_0 in order to let the theoretical and the linearized fit run through zero. In that manner the errors in the low- Q range are suppressed and better results for the straight line with respect to the entire range of the quality factor, and respectively of the settling time, are reached. Additionally a constant relative error between the linearized straight of the measured values and the theoretical line, which is more meaningful for the user, can be achieved since both lines are crossing the origin. This method is acceptable since the important boundary for a minimum value of the settling time $t_{s,min} = 50\mu s$ is established.

8.5 High pass (high-Q) filter measurements

The first question to answer is if the settling time of the different filters is proportional to the quality factor Q as predicted in chapter 7.5. The corner frequency was kept as a constant value at $25kHz$. The transfer function of the applied high pass filter is defined as

$$H_{HP}(s, Q) = -\frac{s^2}{s^2 + \frac{2p \cdot 25kHz}{Q} + 4p^2(25kHz)^2}. \quad (8-16)$$



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Figure 8-5 Settling behavior of high pass filter at corner frequency of 25kHz

Figure 8-5 shows the measured data of the settling times of the high pass (high-Q) filter with the corner frequency of $\omega_0 = 25kHz$. The solid line is the linearized straight line of the data using the method of linear regression. This linear fit of the measurements and the

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theoretical straight, which is represented by the dotted line, are in good agreement with each other. The standard error of estimate $s_{Y,X}$ is a good measure of the variability on average of the measured points about the linearized fit and was found to be $s_{Y,X}=42.5\mu s$. The relative error of the measured (solid) line with respect to the theoretical values (dotted line) is defined as:

$$E_{rel}(Q) = \frac{\|t_{s,theor}(Q) - t_{s,lin}(Q)\|}{t_{s,theor}(Q)} * 100\% , \quad (8-17)$$

where $t_{s,theor}(Q)$ is the theoretical (using equation (7-16)) value for the settling time for a specific quality factor Q and $t_{s,lin}(Q)$ the appropriate measured value after linearization with the method of linear regression. This error is constant over the full range of the varying quality factor because it is determined by (8-17), the difference between the two straight lines that are both crossing the origin. The value for the relative error of the measurements of Figure 8-5 was calculated to be $E_{rel}=2.05\%$.

As the next step we performed measurements with different randomly chosen filters. Figure 8-6 shows the measured values for a high pass (high-Q) biquad, with a corner frequency of $f_0=100kHz$ and varying quality factors Q .

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Figure 8-6 Settling behavior of a high pass filter at corner frequency of 100kHz

In this graph a range of only $300\mu\text{s}$ for the settling time is used. The discrepancies of the data to its linearized straight are small and both straight lines, the linear fit of the data and the theoretical, are almost equal. Thus, the data is matching the theoretical curve very well and the standard error of estimate of these measurements is very small: $s_{Y,X}=18.8\mu\text{s}$ and the relative error of the linear fit is $E_{rel}=0.55\%$.

Additionally, Figure 8-5 shows that the measured values for $Q=1$ and $Q=2$ are much higher than the expected data and stay above the minimum boundary of $t_{s,min}=50\mu\text{s}$.

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8.6 Low pass (high-Q) filter measurements

The transfer function of the used filter (with a corner frequency of 25kHz) is

$$H_{LP}(s, Q) = -\frac{4p^2(25kHz)^2}{s^2 + \frac{2p \cdot 25kHz}{Q} + 4p^2(25kHz)^2}. \quad (8-18)$$

The measurements of this filter are shown in Figure 8-7.



Figure 8-7 Settling behavior of a low pass filter at corner frequency of 25kHz

Figure 8-7 shows that for low corner frequencies, such as $\omega_0=25kHz$ in this example, the range of settling time is very high. Again the data and the prediction are in good agreement with each other. The standard error of estimate amounts to $s_{Y,X}=47.5\mu s$. The relative error between the measured and the theoretical straight line is $E_{rel}=4.51\%$.

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8.7 Band pass (high-Q) filter measurements

The transfer function of the implemented band pass filter ($f_0=10\text{kHz}$) is

$$H_{BP}(s, Q) = -\frac{2p10\text{kHz} \frac{1}{Q} s}{s^2 + \frac{2p10\text{kHz}}{Q} + 4p^2(10\text{kHz}^2)} . \quad (8-19)$$

The measurements of this filter are shown in Figure 8-8.



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Figure 8-8 Settling behavior of a band pass filter at corner frequency of 10kHz

The standard error of estimate $s_{Y,X}$ was determined to be $s_{Y,X}=66.5\mu\text{s}$ and the relative error between the measured and the theoretical straight is $E_{rel}=3.24\%$. The measurements are again in good agreement with the theoretical values.

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The same filter with a different center frequency of $f_0=50\text{kHz}$ was applied to the FPAA and measured. The results are shown in Figure 8-9.

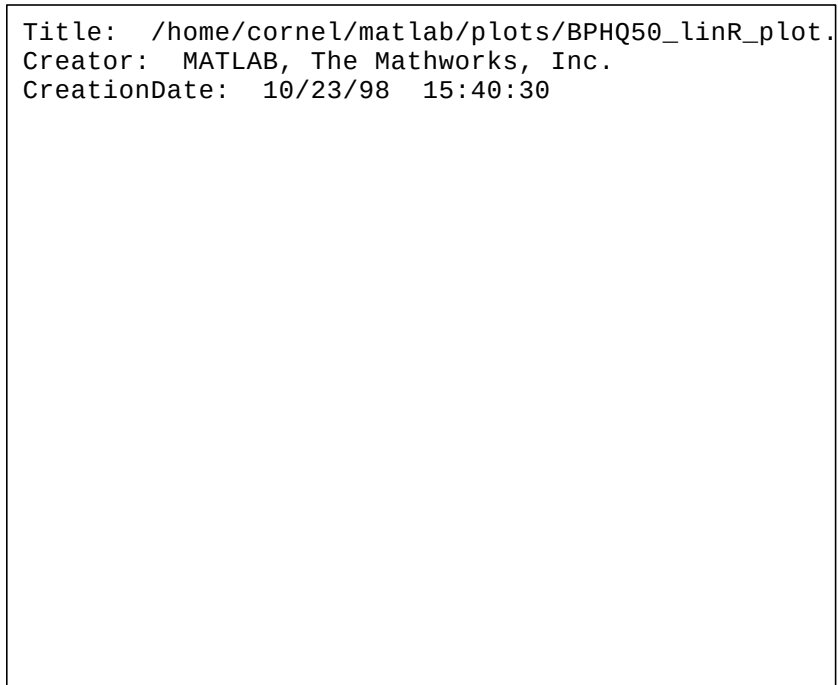


Figure 8-9 Settling behavior of a band pass filter at corner frequency of 50kHz

Figure 8-9 shows measured data that are quite close to its linear fit. Only three points of twenty show higher deviations from the straight caused by reading uncertainties. Therefore the standard error of estimate $s_{Y,X}$ is very small and amounts to $s_{Y,X}=19.7\mu\text{s}$. The relative error of the linear fit of this measurements is $E_{\text{rel}}=1.48\%$. The resulting straight lines are matching well again to each other.

8.8 Band stop (high-Q) filter measurements

The transfer function of the implemented band stop filter with a corner frequency of 50kHz is defined as

$$H_{BS}(s, Q) = -\frac{s^2 + 4p^2(50kHz)^2}{s^2 + \frac{2p \cdot 50kHz}{Q} + 4p^2(50kHz)^2}. \quad (8-20)$$

The measurements of this filter are shown in Figure 8-10.



Figure 8-10 Settling behavior of a band stop filter at corner frequency of 50kHz

Both lines are again in good agreement on each other. The standard error of estimate of this measurements is $s_{Y,X}=21.8\mu s$ and the relative error of the measured straight with respect to the theoretical line is $E_{rel}=1.33\%$.

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Figure 8-6, Figure 8-9, and Figure 8-10 show smaller deviations of the measured points as the other measurements because of the smaller range for the settling time. Therefore the standard errors of estimate $s_{Y,X}$ have smaller values in these cases. The relative error in all these measurements is always below 5% and is mainly caused by reading errors of the oscilloscope because of its low resolution. These results show that the chip behaves as predicted theoretically in chapter 7.5 and that the settling time is proportional to the quality factor of the biquad filter and to the reciprocal value of its corner frequency.

8.9 Effect of additional zeros

We discussed previously in chapter 7.4 the effect of an additional zero in the transfer function of a second-order system on the time response. Let us consider the general transfer functions of a low pass (high-Q) filter as

$$H_{LP}(s, Q) = -\frac{Gw_0^2}{s^2 + \frac{w_0}{Q} + w_0^2},$$

and of a high pass (high-Q) filter as

$$H_{HP}(s, Q) = -\frac{Gs^2}{s^2 + \frac{w_0}{Q} + w_0^2}.$$

The high pass filter has two additional zeros in its transfer function with respect to that of the low pass filter. Therefore, it is important to measure the settling time of these two filters with the same characteristic values and to compare the results. The graphs of the measured data after application of the method of linear regression for linearization of the data are shown in Figure 8-11.

MEASUREMENTS OF SETTLING TIME OF 2ND-ORDER FILTERS



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Figure 8-11 Comparison of systems of 2nd order with and without zeros

The system without zeros (low pass filter, dotted line) needs some more time to settle in. However, this is not in agreement with the theoretical analysis performed in chapter 7.4, where the time response of a system with a zero is defined as the superposition of the time response of same system without a zero and a pronounced early peak as shown in Figure 7-3. This early peak can be achieved by the time derivation of the system time response (without zero), divided by the absolute value of the zero as already presented in equation (7-12). Thus, it is expected that the settling time would increase if there is an additional zero in the transfer function.

However, the differences between the transfer functions shown in Figure 8-11 are quite small in comparison to the reading errors and measurement uncertainties of settling time in general and therefore within experimental errors. The linear dependency of the settling time on the quality factor and on the reciprocal value of the corner frequency is

MEASUREMENTS OF SETTLING TIME OF 2ND-ORDER FILTERS

recognizable. Therefore, these differences are negligible for the determination of the settling time and an additional zero does not essentially effect the settling behavior.

9. FILTERS OF HIGHER ORDER

9.1 Cascading Biquads

In practice, filters of higher order are commonly used because of their better performance of the filter behavior, such as in the transition band, which leads from the pass-band edge frequency to the stop-band edge frequency. The difference between the pass-band and stop-band edge frequency is a measure for the sharpness of the filter response and can usually be improved by a system of higher order. The easiest way to implement such a filter of higher order onto the FPAA is to cascade several blocks of filters of first or second order. The FPAA contains 20 operational amplifiers and due to the equal number of integrators it is possible to realize a filter of 20th order on one FPAA.

It is also necessary to investigate the settling behavior of these filters to develop a model for the prediction of the time delay that is needed for the reconfiguration process. Because of mathematical limits it is not practical to analyze theoretically the time response of any system of higher order as performed in chapter 7 for systems of second order.

9.2 Overshoot effect of cascading identical high-Q biquads

The transfer function of a High pass high-Q biquad filter is defined as:

$$H_{high\,pass}(s) = - \frac{G s^2}{s^2 + \frac{w_0}{Q} s + w_0^2} . \quad (9-1)$$

FILTERS OF HIGHER ORDER

Cascading biquad filters means that the transfer functions of (9-1) are multiplied with each other. It is interesting to have a look on the pass band magnitude at the corner frequency ω_0 , at which the peak of the magnitude response occurs. The absolute value of $H_{high\ pass}(s)$ at $s=j\omega_0$ is:

$$|H_{highpass}(\omega_0)| = \left| -\frac{G(j\omega_0)^2}{(j\omega_0)^2 + \frac{\omega_0}{Q} j\omega_0 + \omega_0^2} \right| = \left| -\frac{-G\omega_0^2}{-\omega_0^2 + j\frac{\omega_0^2}{Q} + \omega_0^2} \right| = GQ . \quad (9-2)$$

The gain G was set to the value of one for all filters, but if Q is bigger than the value of one a higher value at the corner frequency with respect to the input signal is obtained. This effect is called overshoot peak of the magnitude. The overshoot peak is characterized by the value of the quality factor Q . When a filter of n^{th} order is generated by cascading $n/2$ biquads with identical corner frequencies, the absolute value of the magnitude response at the corner frequency can be determined by multiplying (9-2):

$$|H_n(\omega_0)| = \prod_{i=1}^{n/2} Q_i \quad (9-3)$$

That means for quality factors of $Q>1$ there may be a significant amplification of the input signal. In this study we performed measurements on a filter of 20^{th} order with a quality factor of $Q=3$ and achieved a sinusoidal output signal with the frequency of $\omega=\omega_0$, even when the input pin was grounded. Therefore, the filter selected the corner frequency out of the noise background and amplified it by $|H(\omega_0)|=3^{10}$ times, such that there was a signal visible on the oscilloscope. In order to avoid this effect biquad blocks with low quality factors ($Q\leq 1$) were applied for the measurements described below.

9.3 Measurements on cascaded biquad filters

As a first experiment we measured the settling time of a series of increasing order of filters, generated by cascading identical high pass biquads. In other words, first a filter of 2nd order was used, then a filter of 4th order, built by 2 biquads, afterwards a 6th-order filter by three identical biquads, and so on up to a filter of 20th order, built by ten cascaded high pass biquads. For each of these filters the settling time was measured with varying corner frequencies. A quality factor of $Q=1$ was used.

Figure 9-1 shows the results of measuring filters of 4th order (lower curve), 10th order, and of 20th order (upper curve).

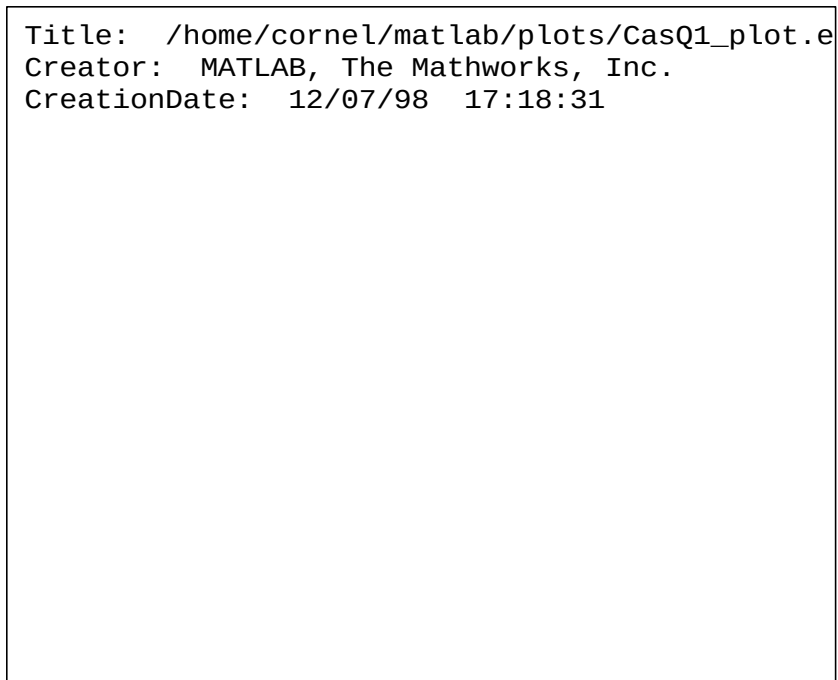


Figure 9-1 Settling time of filters of 4th order, 10th order, and 20th order

FILTERS OF HIGHER ORDER

Figure 9-1 shows that the settling time of a system of higher order is, as in a 2nd-order system, proportional to the reciprocal value of the corner frequency and differs from filters of smaller order with an offset. This is analogous to the theoretical predictions and measured results for the settling time of a particular biquad shown in the previous sections.

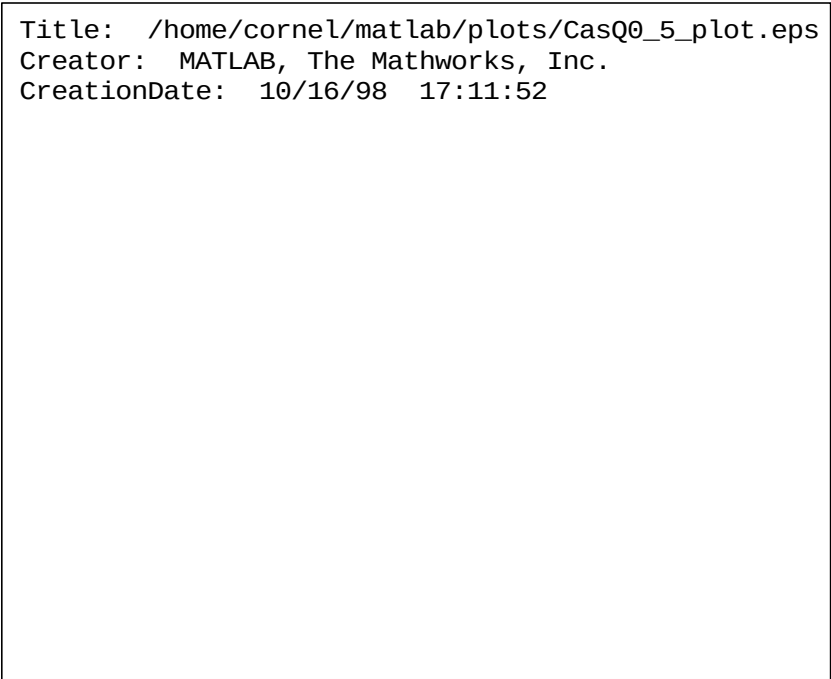
The results for another measurement series, using biquads with a quality factor of $Q=0.707$, are shown in Figure 9-2:



**Figure 9-2 Settling behavior of cascaded filters ($Q=0.707$) from 2nd- up to 20th-
order**

The equivalent measurements for cascaded biquads with $Q=0.5$ are illustrated in Figure 9-3. The curve with the biggest settling time values corresponds to the system of 20th order and that with the smallest values to the 2nd order system in both figures.

FILTERS OF HIGHER ORDER



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Figure 9-3 Settling behavior of cascaded filters ($Q=0.5$) from 2nd up to 20th order

These three figures show that for low corner frequencies the settling time increases rapidly and for a range higher than about 70kHz the settling time is almost constant around $t_s=50\mu\text{s}$. Therefore, in the high frequency range ($f>60\text{kHz}$) the settling time of a cascaded (low Q) biquad filter can be assumed to be constant and the time delay can be predicted as the minimum value of $t_{s_min}=50\mu\text{s}$. Various measurements with low Q -biquads in high frequency range done in order to get the minimum possible settling time of a filter implemented on the FPAA indicated that the value of $t_{s_min}=50\mu\text{s}$ is the shortest time that can be reached to get the signal into a steady-state shape. Comparing the ranges of the settling time of the three graphs they show also that for higher quality factors Q the settling time increases linearly. This is analogous to the theoretical predictions shown in the previous sections.

9.4 System with dominant poles

The results presented in chapter 7 are true for systems of second order. These results can be extended to systems of higher order with one dominant pair of complex poles [Nagrath 1975], that is one pair of poles very close to the $\mathfrak{J}$ -axis. These dominant poles specify the time response of the system as long as their real part is much smaller than that of the other poles. In that case the non-dominant poles can be neglected and the time response of the system of higher order can be approximated by a system of second order with respect to the settling behavior. The problem is now to find a minimum boundary for the ratio of the non-dominant to dominant poles above which it is possible to neglect the non-dominant poles and to handle the system by the time response of a second-order system. Let us consider, as an example, a third-order system with a closed-loop transfer function:

$$H_{third-order}(s) = \frac{w_0^2}{s^2 + \frac{w_0}{Q}s + w_0^2} \left(\frac{2}{p_n} + 1 \right) \quad (9-4)$$

FILTERS OF HIGHER ORDER

The complex pair of poles can be obtained by:

$$p_{d_{1/2}} = -\frac{w_0}{2Q} \pm \sqrt{\frac{w_0^2}{4Q^2} - w_0^2} = -\frac{w_0}{2Q} \pm jw_0 \sqrt{1 - \frac{1}{4Q^2}} \quad \forall Q > 0.5. \quad (9-5)$$

So the real part of the poles is defined as $\Re\{p_d\} = -\frac{w_0}{2Q}$ and if

$$p_n \geq 10|\Re\{p_d\}| = 10\frac{w_0}{2Q} \quad (9-6)$$

[Nagrath 1975], the transfer function $H_{third-order}(s)$ can be approximated by a second-order system with the transfer function

$$H_{approx.}(s) = \frac{w_0^2}{s^2 + \frac{w_0}{Q}s + w_0^2}. \quad (9-7)$$

The relative location of the dominant poles (p_d) of this system with respect to the other (neglected) pole (p_n) is illustrated in Figure 9-4:

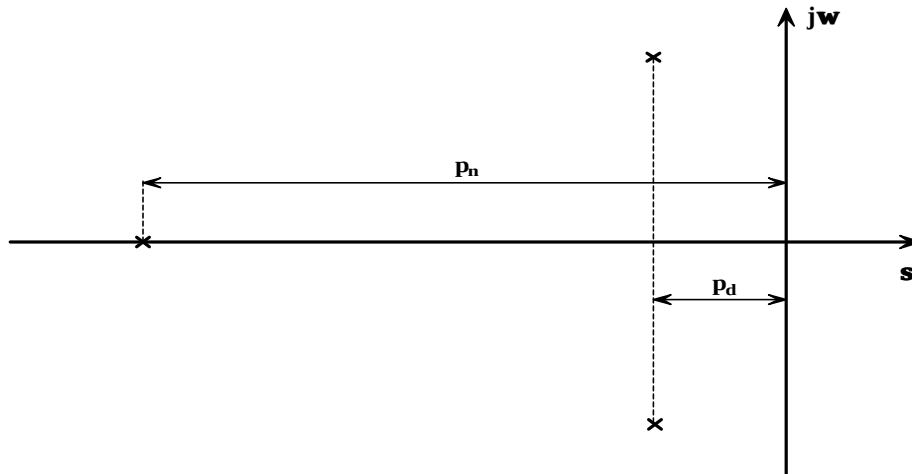


Figure 9-4 Location of poles of the 3rd-order system

FILTERS OF HIGHER ORDER

To prove (9-6) measurements are necessary that vary the ratio of the real parts of non-dominant to dominant poles in order to find the boundary above which it is possible to neglect the non-dominant poles. Figure 9-5 shows the results of measurements of low pass (high-Q) filter of different orders, established by cascading biquads, with varying ratios R_{pole} of the non-dominant (all identical) to the dominant poles:

$$R_{pole} = \frac{|\Re\{p_n\}|}{|\Re\{p_d\}|} \quad (9-8)$$

The variation of the poles was performed by choosing different corner frequencies, since the real part of the pole is proportional to the corner frequency of the appropriate biquad block as shown in (9-5). The pair of dominant poles was constant for all measurements.

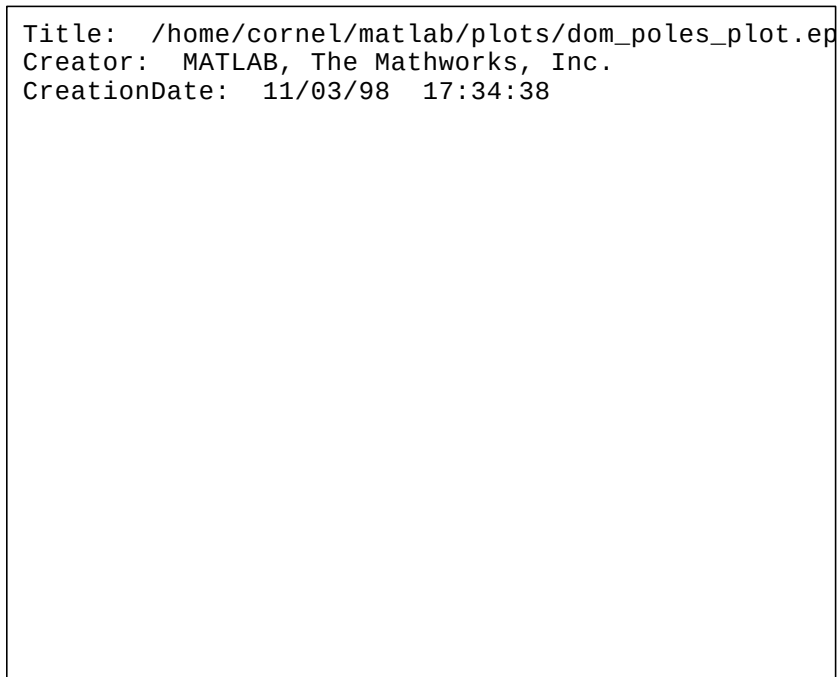


Figure 9-5 Settling behavior of systems with dominant poles

FILTERS OF HIGHER ORDER

Figure 9-5 shows that poles that are located close to the dominant pair have a high influence on the time response and increase the settling time significantly. This influence disappears above a minimum ratio of non-dominant to dominant poles:

$$R_{\min} = 4. \quad (9-9)$$

Therefore, the bigger the real parts of all the non-dominant poles are, with respect to the dominant poles, the smaller is the influence they have on the settling behavior. And if the ratio R_{pole} is bigger than $R_{\min} = 4$, the settling time of the system of higher order is almost equal to the second-order system. However, the measurements in this section show that all higher-order systems with dominant poles have a little higher values for the settling time in comparison to the second-order systems for ratios $R_{pole} > R_{\min} = 4$. This offset for the settling time is constant as shown in Figure 9-5 and is several dimensions smaller than the influence of the poles located close to the dominant pair. This effect should be considered when the time delay for a system of higher order is determined, especially with an implementation of a system of 10th order or higher due to the consideration of bigger offsets at a higher number of poles.

10. SUMMARY

10.1 *Conclusions*

A concept of dynamic reconfiguration of analog filters, using two parallel Field Programmable Analog Arrays (FPAAs) controlled by a digital system and switched by a multiplexer, is presented in this work. The FPAA, built in switched-capacitor technology, is a device for fast design and prototyping of analog circuits of high flexibility and easy handling using the provided software EasyAnalog™. The switching of the multiplexer was controlled by a digital circuitry that reacts on a control signal generated after the reconfiguration phase of the FPAA. Switching perturbations were analyzed and explained in detail. Quantities such as the settling behavior of the reconfigured FPAA after the switching and the signal discontinuities during multiplexing were studied. In order to provide a basis for ‘hiding’ the settling behavior, theoretical investigations about the time response in systems of second-order, represented by biquad filters implemented on the FPAA, were carried out and a model for the time delay of switching was established. The effect of additional zeros in the transfer function and its modeling were also discussed. The model for the settling time was confirmed with measurements of all types of filters. For comparison of the measured values with the theoretical curve, the method of linear regression was used for the measured data in order to achieve a more meaningful representation of the measurements. During the measurements it was discovered that the settling time has a certain minimum time boundary that has to be provided as a minimum time delay for the switching in general. The measurements indicated that the FPAA exhibits the discussed settling behavior predicted by the theoretical investigations. The developed model can be used for the determination of the time delay at the switching moment. Using this model of the settling time it is possible to generate the proper time delay for the

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switching to obtain the output signal without undesired switching perturbations. The model was extended to systems of higher-order, such as cascaded second-order filters or systems with dominant poles, where it is possible to neglect the effect of non-dominant poles and to handle the filter as a second-order system with a time response determined by the pair of dominant poles. Measurements showed that above a certain ratio of non-dominant to dominant poles the settling time can be determined using the established model for second-order systems. All the measurements of systems of higher-order showed the direct dependency of the settling time on the characteristic parameters of the different filters, such as corner frequency and quality factor. This model of the settling time can now be used to implement a digitally controlled time delay into the FPGA which replaces the controlling task of the PC and the switching part of the multiplexer, as previously discussed in chapter 4.1. Having a model of the time delay for the desired filter function, it is possible to develop a method for optimization of the multiplexing process and for minimization of the switching perturbations and the reconfiguration time .

10.2 Future Outlook

The main purpose of these investigations was to develop the model for the settling behavior of the signal in the FPAA and for the switching perturbations in order to include this information into a more sophisticated system, where the entire controlling will be done by one digital block. This controlling device could be realized using a Field Programmable Gate Array (FPGA). Using a FPGA for controlling the reconfiguration and the multiplexing might have many advantages. It is expected that the reconfiguration time of the FPAA will be reduced significantly, maybe by several orders of magnitude, from the current programming time of approximately 3s, if the FPAA is programmed by a FPGA instead of

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a PC via the serial communication port. Additionally, it is possible to include an ‘intelligent’ (digital) time delay model into the FPGA, which determines the specific time delay depending on the different filters as presented in the previous sections, in order to ‘mask’ the settling curves and provide an output signal without switching perturbations. Another task of the FPGA could be the analysis of the input signal in order to program the desired filter function onto the processing chips as well as monitoring of the processed output signal for a fast reconfiguration. For this reason there should be feed-back and feed-forward branches to provide the FPGA with the needed information, as already mentioned in chapter 4.1. With the information of the input signal it should also be possible to detect the zero-crossing of the sinusoidal input signal and to set the switching moment exactly into the zero-passing of the signal (in case of changing the quality factor) in order to minimize high frequency components as previously discussed in chapter 5.2. However, a big disadvantage of the analog filtering by the FPAA is that it cannot provide the high-accuracy and high-complexity signal processing algorithms which are typically possible in digital circuits. To avoid this drawback it is desirable to extend the system to high-complexity filtering by including a digital part for digital signal processing. On this account it is desirable to establish two additional FPGA that work in parallel in order to provide dynamically reconfigurable digital processing devices. That system would include two FPAAs and two FPGAs, all established in parallel, and the main FPGA which controls the signal processing by programming the desired chip and by multiplexing between the four outputs of the chips.

The block diagram of that system is shown in Figure 10-1:

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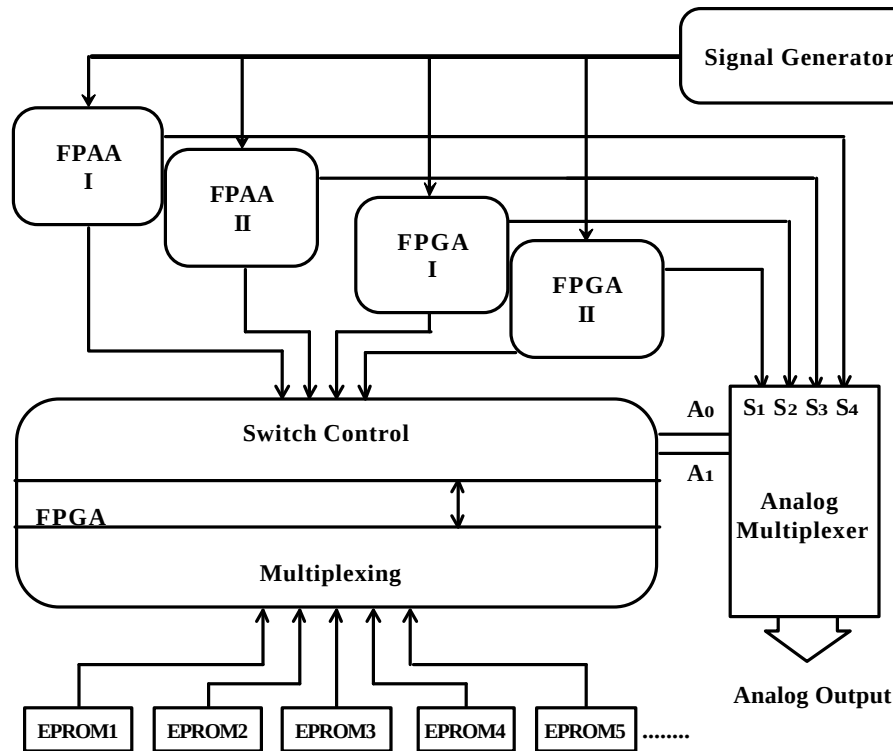


Figure 10-1 FPAA/FPGA dynamic reconfiguration system

Using the digital part of the system a digital high-order filter can be created with high accuracy. On the other hand the analog part is suitable for high-speed processing with lower power consumption. Instead of building up a slow software that requires a high amount of memory like EasyAnalog™, which runs on the PC as presented in chapter 3.2, it would be advantageous to store the data for all kinds of different filters into memory. This memory could be realized by EPROMs that should be accessible by the main FPGA. In order to minimize the reconfiguration process of the chips the main FPGA can choose the data of the desired filter function by multiplexing between the different EPROMs. Therefore, a high reconfiguration rate can be accomplished, if the input signal changes permanently and if there is a need for current ‘adaptive’ filtering. This system, which is

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able to provide digital and analog signal processing, would be a very suitable device for many different purposes in modern applications, where power dissipation, mobility and level of accuracy is important.

11. APPENDIX

11.1 The used hardware components

Table 2 shows the electronic components that were used to build up the control board.

Table 2 Denotation of the used devices

U₁	DG 406 Multiplexer
U₂, U₃	7400 Quad 2-Input NAND Gate
U₄	74132 Quad 2-Input NAND Schmitt trigger
U₅, U₆, U₈	74123 Retriggerable monostable Multivibrator
U₇	74HCT132 Quad 2-Input NAND Schmitt trigger

The **DG406 Multiplexer**, noted as U1, is a 16-channel single-ended analog multiplexer that is designed to select one of sixteen inputs to a common output as determined by a 4-bit binary address that is entered to four address input pins. The device works equally well in both directions. Additionally to the 16 input, 1 output, and 4 address pins the chip has an enable pin for resetting all switches and functions. All digital control inputs are TTL compatible over the full specified operating temperature range.

The features of the DG406 include:

- Low On-resistance $r_{DS(on)}=50\Omega$
- Low charge injection $Q=15pC$
- Fast transition time $t_{trans}=200ns$
- Low power $P=0.2mW$
- Wide supply ranges: $\pm 5V$ to $\pm 20V$

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Applications of the DG406 are high speed data acquisition, audio signal switching and routing, ATE systems and avionics. High performance and low power consumption make them suitable for mobile, battery-operated systems. [TEMIC 1997].

The components noted as U2 and U3 are **7400** Quad 2-input NAND gates that were used to build up the flip-flop. On one chip four NAND Gates are included, every gate with 2 inputs. The supply voltage for these components, equal to all the other components except the multiplexer U1, is 5V.

U4 is a **74132** Quad 2-Input NAND gate with Schmitt-trigger inputs and contains four 2-input NAND gates like the 7400. The devices are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals for dynamic stabilization of the binary levels. In addition, they have greater noise margins than conventional NAND gates, as for example the **7400**. Each circuit contains a 2-input Schmitt-trigger followed by a Darlington level shifter and a phase splitter driving a TTL totem-pole output. The Schmitt-trigger uses positive feedback to effectively speed up slow input transitions to sharp peak changes and to provide different input threshold voltages for positive- and negative-going transitions. This hysteresis between the positive-going and negative-going threshold is determined by (internal) resistor ratios and is insensitive to temperature and supply voltage variations [MOTOROLA 1995].

The **74HC123**, denoted as U5, U6, and U8, are dual retriggerable monostable multivibrators with output pulse width determination by three methods. The basic pulse time is programmed by selection of an external capacitor C_{ext} and resistor R_{ext} . The connections of these external components are shown in Figure 11-1:

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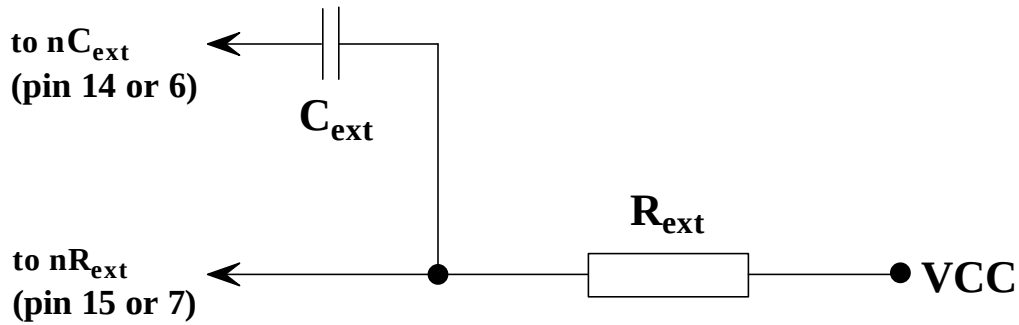


Figure 11-1 Timing component connection of the 74123

Once triggered, the basic output pulse width may be extended by retriggering the gated active LOW-going edge input ($n\bar{A}$) or the HIGH-going edge input (nB). By repeating the process, the output pulse period ($nQ=HIGH$, $n\bar{Q}=LOW$) can be made as long as desired. Alternatively an output delay can be terminated at any time by a LOW-going edge on the input $n\bar{R}_E$, which also inhibits the triggering.

An internal connection from $n\bar{R}_E$ to the input gates makes it possible to trigger the circuit by a positive-going signal at the input $n\bar{R}_E$. The basic output pulse width is essentially determined by the external components C_{ext} and R_{ext} . For $C_{ext} > 10nF$ the typical output pulse width can be determined as [PHILIPS 1998]:

$$t_w = 0.45 * R_{ext} * C_{ext}$$

where:

- t_w = pulse width in ns;
- R_{ext} = external resistor in $k\Omega$;
- C_{ext} = external capacitor in pF;

as already discussed in chapter 4.2.

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Additionally, Schmitt-trigger action in the $n\bar{A}$ - and nB -inputs makes the circuit highly tolerant to slower input rise and fall times, as discussed previously in the regard to the **74132**.

U7 is a **74HCT132** Quad 2-Input NAND gate with Schmitt-trigger inputs and provides the same function and performance as the **74132**, which is deployed as U4. The only differences exist in the different ranges of input voltages and other performance options.

The layout of the board is shown in Figure 11-2:

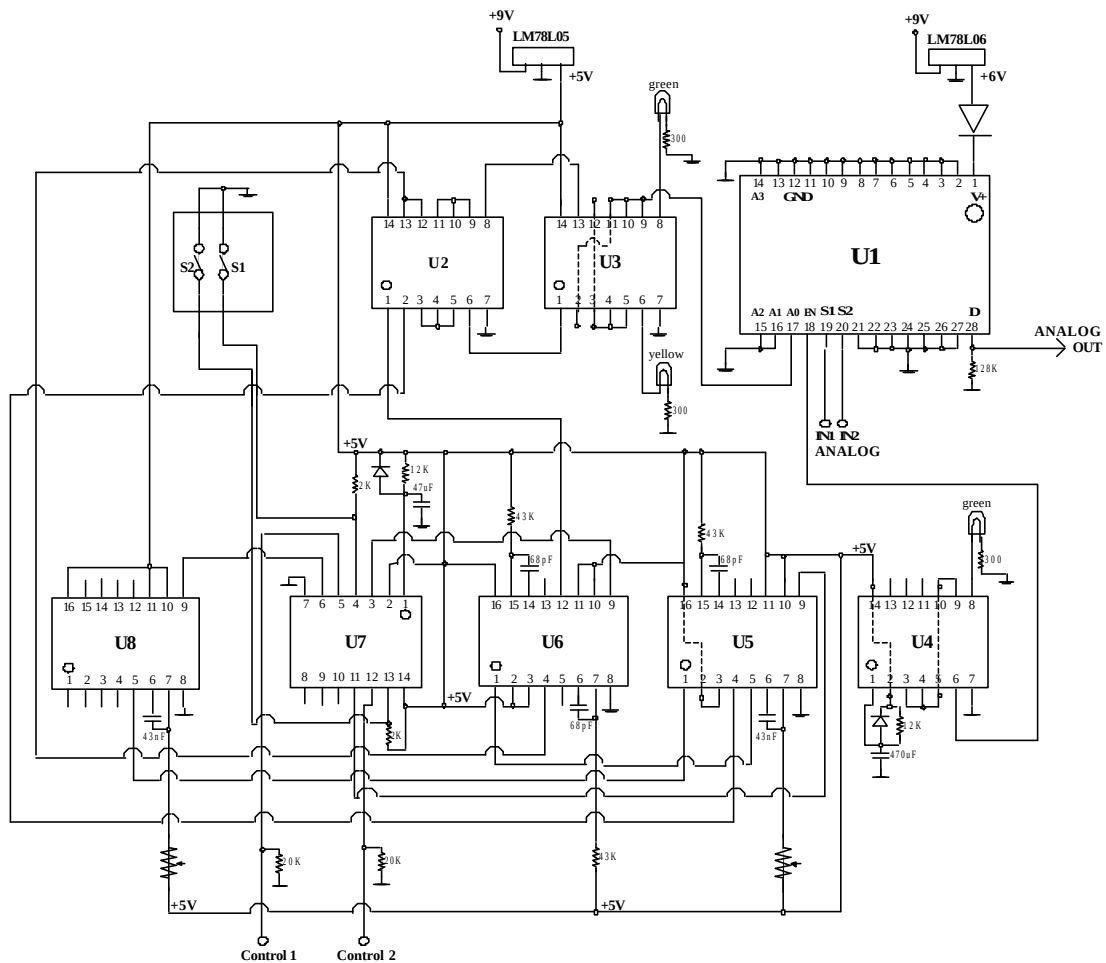


Figure 11-2 Control board layout

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The power supply was established using two voltage regulators, a **LM78L05** and a **LM78L06 3-Terminal positive regulator**, which transfer the voltage from 9V down to 5V and 6V respectively. Applying fixed output voltages with tolerances of $\pm 5\%$ over the temperature range [NATIONAL SEMICONDUCTOR 1995], the regulators are very useful in providing a stable voltage source. The main 9V-source was established by two AC-adapters that transfer the *110V, 60Hz AC* from the wall outlet to the *9V DC*.

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