1) We wish to build an up/down counter (3 bits) out of JK-flip-flops. If the input \( I = 0 \), the counter counts up from 0 to 7, then repeats. If \( I = 1 \), the counter counts down from 7 to 0, then repeats.

a) Draw the state diagram of this counter.

b) Provide the state transition table.

c) Use Karnaugh maps to design the combinational logic circuit.

d) Draw an implementation using a PLA for the combinational logic.
2) A digital-to-analog converter converts a binary number into an equivalent voltage, e.g.

<table>
<thead>
<tr>
<th>Q2 Q1 Q0</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0</td>
<td>0 V</td>
</tr>
<tr>
<td>0 0 1</td>
<td>1 V</td>
</tr>
<tr>
<td>0 1 0</td>
<td>2 V</td>
</tr>
<tr>
<td>0 1 1</td>
<td>3 V</td>
</tr>
<tr>
<td>1 0 0</td>
<td>4 V</td>
</tr>
<tr>
<td>1 0 1</td>
<td>5 V</td>
</tr>
<tr>
<td>1 1 0</td>
<td>6 V</td>
</tr>
<tr>
<td>1 1 1</td>
<td>7 V</td>
</tr>
</tbody>
</table>

It can be easily built using a resistive network.

A comparator compares two analog voltages, and puts out a digital number (1 bit).
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\[ \begin{array}{ccc}
\mathbb{R}_1 & \rightarrow & \text{Comp} \\
\downarrow & & \downarrow \\
\mathbb{R}_2 & \rightarrow & 0 \\
\end{array} \]

e.g. \[ \begin{array}{ccc}
\mathbb{Z}_1, \mathbb{Z}_2 & | & 0 \\
\mathbb{Z}_1, > \mathbb{Z}_2 & | & > \\
\mathbb{Z}_1, < \mathbb{Z}_2 & | & 1 \\
\end{array} \]

It can be easily built using an operational amplifier.

We wish to construct an analog-to-digital converter:

\[ \begin{array}{ccc}
\mathbb{Z} & \rightarrow & \mathbb{N} \\
\downarrow & & \downarrow \\
\text{#} & \rightarrow & \mathbb{G} \\
\end{array} \]

using:
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→ one digital-to-analog converter
→ one comparator
→ one 3-bit up/down counter

\[ I \rightarrow \uparrow \downarrow \rightarrow Q \]

i.e., the circuit designed in problem #1.

Draw the circuit that implements the analog-to-digital converter.
3) We want to design a 3-bit shift register using D-flip flops. The shift register can either shift to the right \((M = 0)\), or to the left \((M = 1)\). If \(M = 0\), the input \(I\) shifts from left into \(Q_2\). If \(M = 1\), the input \(I\) shifts from right into \(Q_0\).

a) Provide the state transition table.

b) Using Karnaugh maps, design the combinational logic circuit.

c) Draw the circuit implementing this shift register.
4) We want to build a 5-bit digital function generator. 5 inputs describe the sequence of outputs to be seen, e.g.

\[ I = \langle \phi 1 \, 1 \, \phi 1 \rangle \]

\[ \Rightarrow O = \phi 1 \, 1 \, \phi 1 ; \phi 1 \, 1 \, \phi 1 ; \phi 1 \, 1 \ldots \]

The output repeats itself.

We use a 5-bit circular shift register with parallel load. A control input \( M \) is used to decide whether we shift or load:

\[ M = 0 \ : \ \text{shift} \]
\[ M = 1 \ : \ \text{load} \]

Use D-flip flops to design the circuit.