1) Make a T-flip flop out of a D flip flop. You are allowed to use only one combinational gate beside from the D flip flop.

2) Given the master-slave flip flop of Fig. 6.22:

![Diagram of master-slave flip flop]

Figure 6.22 Schematic for J-K master/slave flip-flop.

Design combinational hardware around it that will accomplish the following:
Add a high-active asynchronous enable input. If disabled, neither the master nor the slave will change their state values.

Add a low-active synchronous clear input. If set, both the master and the slave will be reset to zero at the next clock. In accordance with the normal operation of the flip-flop, the master will reset when the clock goes high, whereas the slave will reset, when the clock goes low.
3) Design circuitry to implement the following Gray-code counter:

Using 3 JK-flip-flops. Ensure that the counter is self-starting.

4) a) Build a counter that counts up from 4 to 11, then repeats. Use a 74163 chip plus additional combinational logic as needed.
Let's examine a counter component from the TTL catalog. Figure 7.12 shows the schematic shape of the TTL 74163 synchronous 4-bit counter. The component has four data inputs, four data outputs, four control inputs (P, T, LOAD, CLR), one control output (RCO), and the clock.

When the LOAD signal is asserted, the data inputs replace the contents of the counter's internal flip-flops. Similarly, when CLR is asserted, all the flip-flops are reset to zero. These operations are synchronous. Although the load or clear signal must be asserted before the clock edge, the actual operation occurs on the positive transition of the clock. Contrast this with asynchronous operation, in which the load or clear takes place as soon as the appropriate control signal is asserted. We will say more about synchronous versus asynchronous counter operation in Section 7.5.

The P and T inputs cause the counter to advance to the next state in the binary sequence when both are asserted. Again, the count operation takes place when the clock undergoes a low-to-high transition. RCO is a ripple carry output that is asserted after the same rising clock edge that advances the counter to its largest value, 1111. This signal can be used as a count enable signal to a second cascaded counter (see Section 7.5.1).

b) Modify the circuit, such that it counts down from 11104, then repeats.

5) Build a circuit that computes the binary square numbers from 0 to 49 (like our Lab #5). This time, we want to use:

1x 74163 (up counter)
6x 74151 (8:1 mux)