ECE 274
2nd Midterm
Monday, March 25, 2002

1) Given the function:

\[ F(A, B, C, D) = \Sigma m(1, 3, 5, 6, 7, 9, 12, 13, 14) + d(4, 8) \]

Find an all-NAND implementation that is free of static hazards of both types.

2) We want to build a very simple ALU:

<table>
<thead>
<tr>
<th>S, S_0</th>
<th>F</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0</td>
<td>A \cdot B</td>
</tr>
<tr>
<td>0 1</td>
<td>A + B</td>
</tr>
<tr>
<td>1 0</td>
<td>\overline{A \cdot B}</td>
</tr>
<tr>
<td>1 1</td>
<td>A \oplus B</td>
</tr>
</tbody>
</table>
a) Use one 4:1 mux plus additional gate logic as needed. Only 2-input NAND gates are available. Minimize the number of 7400 chips needed to implement the additional gate-level logic.

b) Replace the mux by high-active tri-state buffers. Redraw the complete circuit.

3) We want to build a masking circuit
The masking circuit operates as follows:

\[ X_i = A_i \]

except if the address, composed of \( S_i \) and \( S_0 \) selects the element \( i \). In that case:

\[ X_i = \emptyset \]

Hence, the address masks out one of the four bits, and sets it to zero.

a) Find Boolean expressions for the four outputs \( X_i \).

b) Implement the circuit using transmission gates.
4) Given the following 12-bit 2-complement binary number:

100100101100

a) Find the decimal value of that number.

b) Find the hexadecimal value of that number.

5a) Draw a 4-bit adder/subtractor circuit for 2-complement binary numbers. The circuit uses XOR gates for the select function (to distinguish between addition and subtraction). It also uses a carry-look-ahead circuit.
b) After how many gate delays will the sum/difference be available for readout, assuming that all logic gates have comparable gate delays?
6) Given the circuit:

\[ S \quad Q_1 \quad Q_2 \quad R \]

a) Show the complete state transition diagram of this circuit.

b) Can this circuit be used as an RS-latch?

c) If the answer to (b) is positive, which combination of inputs would you have to forbid?