1) Given the following 6-variable Karnaugh map:
2) Given the Boolean function:

\[ F(A,B,C,D) = \Pi M(\emptyset, 7, 9, 13, 14) + \Sigma d(1, 4, 5, 15) \]

a) Use the Quine-McCluskey algorithm to design a minimal 2-level logic realization in product-of-sum form.

Hint: Find a sum-of-product form for \( \overline{F} \) by going after the Os and the Xs, ignoring the 1s. Then convert to the desired product-of-sum form for \( F \).
b) Draw a realization of your function \( f \) using AND and OR gates, as well as inverters.

c) Convert to all-NOR logic.

3) Given the following 4-variable Karnaugh map:

Find a minimal 2-level logic realization in Sum-of-Product form that is free of 0- and 1-hazards.
4) Given the following Boolean function:

\[ F(A, B, C, D) = \Pi M(0, 1, 5, 7, 11, 12) \]

We want to build an MSI circuit for this function. We have available the following two chips:

![Diagram of two MSI chips]

a) We use A and B as address bits for the Mux. Hence we write down the truth table of the function and split it into four parts of equal sizes, such that A and B are constant in each slice.
b) We find logic expressions for the four maps from C and D into F:

<table>
<thead>
<tr>
<th>C</th>
<th>D</th>
<th>F_i</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>...</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>...</td>
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<td>1</td>
<td>0</td>
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<tr>
<td>1</td>
<td>1</td>
<td>...</td>
</tr>
</tbody>
</table>

We connect the F_i’s into the 4 inputs of the Mux.

d) We convert the logic circuit to all-NAND logic.

e) Draw the wiring diagram that shows how you need to connect the two chips together.
5) We want to build a system with 4 inputs and 3 outputs:

- If A is zero, then \((X, Y, Z)\) is \((B, C, D)\) incremented by 1.
- If A is one, then \((X, Y, Z)\) is \((B, C, D)\) decremented by 1.

a) Write down the truth table for this system.
b) For the realization of the system, we have available two 3-bit-wide 8-word ROMs and 7400's.

Cut the truth table into two slices of equal size, such that the control signal A is constant in each slice.

Show what needs to go into the two ROMs:

\[ \text{ROM}_1 \quad (A = 0) \]

\[ \text{ROM}_2 \quad (A = 1) \]
c) Assume that the ROMs use tri-state logic. The outputs are floating if the enable signal is high. The outputs show the correct output if the enable signal is low.

Show the wiring diagram for the two ROMs and the NAND-gates.