NAND-NAND LOGIC CIRCUITS

The simplest Boolean form to find through such minimization techniques as the Karnaugh map is the AND-OR form. This can, of course, be realized using AND and OR gates, plus inverters as needed to complement input variables. However, there is often considerable economy to be achieved by using only one gate type for realization. As shown in Sec. 4.2 of the textbook, an AND-OR form can be realized using only NAND gates, replacing both the AND gates and the output OR gate with NAND gates, on a one-for-one basis. For this experiment you have two logic functions to realize. Determine minimal AND-OR designs by using Karnaugh maps, and then wire the circuits using only NAND gates. For these designs you may assume double-rail inputs, i.e., all input variables are available in both the true and complemented form. On the Digi-Designer the four slide switches are the most convenient source of input variables, but they provide only single-rail inputs. At the start, before you wire either circuit, connect four of the inverters in a 7404 chip to the four slide switches. You will then have double-rail signals available for the rest of the experiment. You will have 7400, 7410, and 7420 chips available. Note that you should try to use all the gates on each chip, to minimize the chip count. For example, if you need 9 2-input gates and 2 3-input gates, you can use the extra gate on the 7410 as the ninth 2-input gate, since two inputs tied together function as a single input.

I Multiplier Circuit

This first part of laboratory project #3 calls for the design of a multiple-output multiplier circuit. There will be
four inputs, \(A_1, A_0\) and \(B_1, B_0\). \(A_1\) and \(A_0\) will be interpreted as a 2-bit binary number where \(A_1\) is the high bit. Similarly, \(B_1\) and \(B_0\) will be interpreted as a 2-bit binary number. This circuit will have four outputs, \(Y_3, Y_2, Y_1,\) and \(Y_0\) where \(Y_3\) is the high bit. The four outputs will be interpreted as a 4-bit binary number equal to \(A_1 A_0 \times B_1 B_0\). In other words, you are to design a circuit that multiplies 2, 2-bit numbers.

This problem is equivalent to designing four circuits \((Y_3, Y_2, Y_1, Y_0)\). Show the truth table and Karnaugh maps for each function. (Note that you can determine the result of multiplication using decimal arithmetic and then convert the result to binary.) When you realize the circuits, gates in a single package may be used in separate functions if that is useful in reducing package count. Assume double rail inputs are available. Wire the circuits in all-NAND form and demonstrate their operation to the instructor.

II Priority Network

Given below is a combinational logic network consisting of \(n\) identical components, connected to form a chain. Such networks are called iterative networks. Cell \(i\) has primary input \(A_i\), secondary input \(L_i\), primary output \(Z_i\), and secondary output \(R_i\). It can be seen that \(R_i = L_{i+1}\). Because all cells are identical, only one cell need be designed, provided the desired combinational logic network fits the iterative network model.
An iterative model is to be used in the design of a four input four output priority network. No more than one output of the network is to be 1 regardless of the number of inputs which are 1. The active output (if any) will be the output corresponding to the highest priority input which is 1. Input $A_0$ is the highest priority, input $A_1$ next, etc. Construct a gate level logic diagram for a single cell of your iterative network and include it in your report. Also include Boolean expressions for the primary and secondary outputs.

Construct on your digidesigner in the laboratory a four cell (4 input) priority network. Verify to the laboratory instructor the successful functioning of your circuit for all combinations of values of the four inputs.