1) Verify if the following expressions are true:
   a) \( a \cdot (b \circ c) = (a \cdot b) \circ (a \cdot c) \)
   b) \( a \circ (b \cdot c) = (a \circ b) \cdot (a \circ c) \)

2) Given a combinational circuit with 4 inputs and three outputs:

   \[
   \left< a_3, a_2, a_1, a_0 \right>
   \]
   represents a 4-bit positive digital number in the range 0..15.
$x_2$ is true, iff the input divides integer by 2; $x_3$ is true, iff the input divides integer by 3; and $x_4$ is true, iff the input divides integer by 4. $\phi$ divides integer by any number.

We wish to design this circuit using NAND gates only. Available are:

7400 : 4x 2-input NAND
7410 : 3x 3-input NAND
7420 : 2x 4-input NAND

Find the implementation with the smallest number of chips.
3) Design a circuit implementing the function:

\[ X = \overline{ABC} + \overline{AC} \]

using one 74138 chip:

<table>
<thead>
<tr>
<th>G1</th>
<th>G2A + G2B</th>
<th>C</th>
<th>B</th>
<th>A</th>
<th>Y0</th>
<th>Y1</th>
<th>Y2</th>
<th>Y3</th>
<th>Y4</th>
<th>Y5</th>
<th>Y6</th>
<th>Y7</th>
</tr>
</thead>
<tbody>
<tr>
<td>X</td>
<td>H</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>L</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>H</td>
<td>L</td>
<td>H</td>
</tr>
</tbody>
</table>

and one additional combinational gate. What type of gate do you need?
4) We wish to design a circuit that can divide a 3-bit binary positive number \( a_2, a_1, a_0 \) by a 2-bit binary positive number \( b_1, b_0 \). The result is a division \( x_2, x_1, x_0 \), and a remainder \( y_1, y_0 \).

Example:

\[ 7 : 2 = 3 + 1 \]

\[ 1 \ 1 \ 1 : 1 \ 0 \rightarrow 0 \ 1 \ 1 : 0 \ 1 \]

Division by 0 results in 5 1's as output.
Example:

\[ \Phi = "7+3" \]

\[ 1011 \Phi \Phi = 1111 \]

This is meaningful, because the remainder can never be a 3.

Design the circuit using any technology that you like.

3) We wish to design a sequential circuit with three outputs that generates the following wave forms:

\[ x_2 \]
\[ x_3 \]
\[ x_4 \]
starting with a clock signal of your choice. You may reuse, if you like, any of the circuits already designed before.

6) Using two 74163 ripple counters:

and additional combinational logic as needed, we wish to design an up-counter that counts from 0 to 2Φ and then starts over.
A combination lock with a rotary dial opens if the dial is:

rotated 2 positions to the left
then rotated 1 position to the right
then rotated 1 position to the left
and finally rotated 2 positions to the right.

a) Draw the state diagram of a Mealy machine implementing the control logic of the lock.

b) Show that the state diagram is minimal.
8) Given the following Moore machine:

Reduce this Moore machine to a simpler Moore machine involving a minimal number of states.