ECE 304: Using PSPICE Hierarchical Block Designs

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Hierarchical Block Designs[1]

Cadence PSPICE also allows a block design approach to circuits. For example, a multistage circuit can be shown as a cascade of blocks with input and output leads, and drilling down (descending the hierarchy) exposes the circuit that is inside the box. In this way clutter is reduced and the "big" picture of the amplifier is easier to see. As an example, let's make a two-stage amplifier with a Common Source input stage and a Source Follower output stage. We begin the process as usual, with FILE/NEW PROJECT.

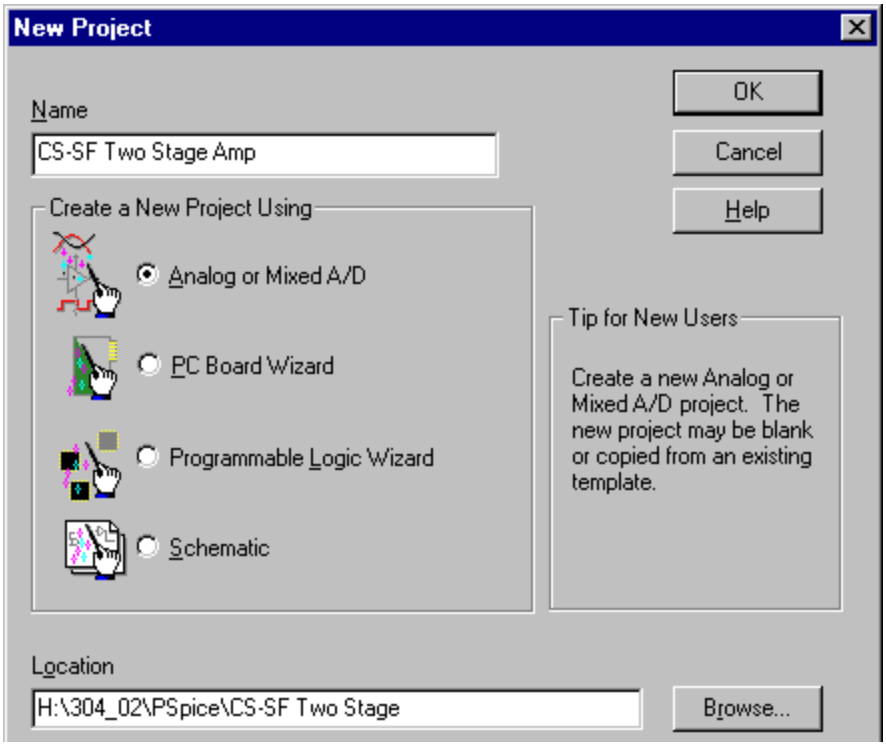

FIGURE 1:
The NEW PROJECT menu: a new folder is created for the project using the BROWSE button.

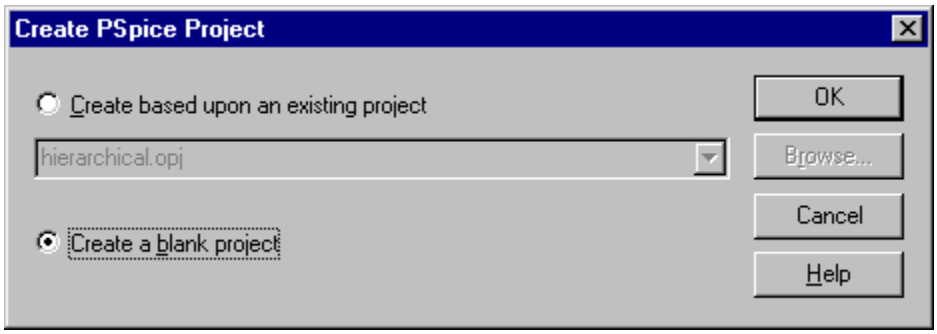

FIGURE 2:
The CREATE PSPICE PROJECT menu. We select CREATE A BLANK PROJECT.

[1] See Herniter's updates at his Web Site, http://www.rose_hulman.edu/~herniter/

Once the project is created, we proceed to place an hierarchical block on the schematic.

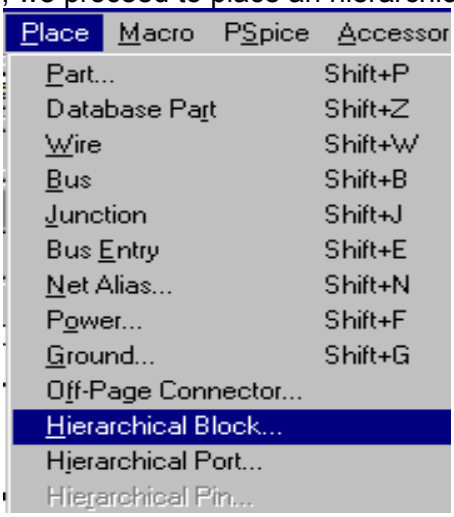

FIGURE 3:

Election to place an hierarchical block

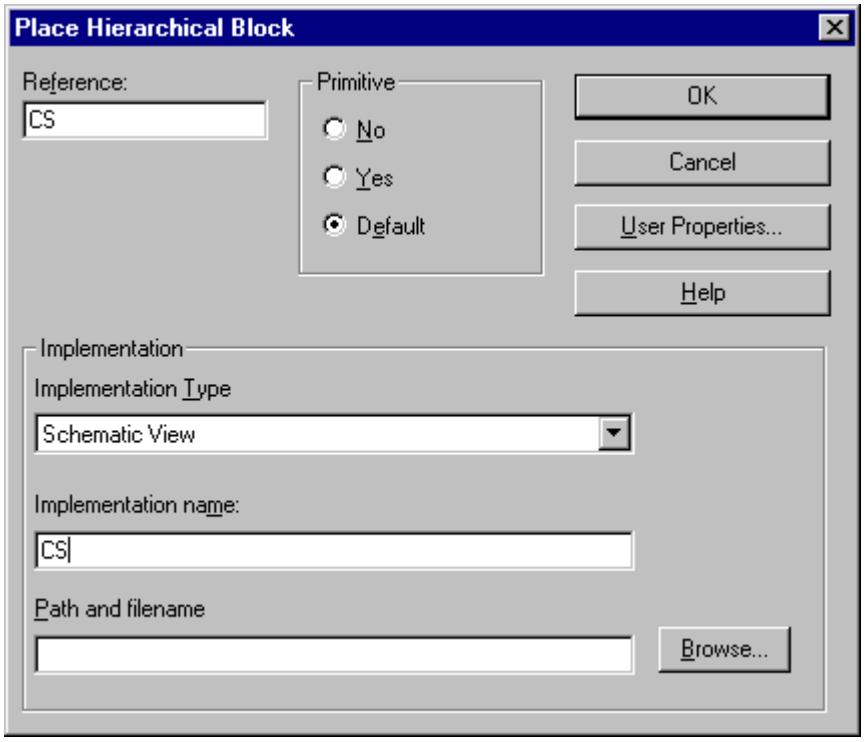

FIGURE 4:

The PLACE HIERARCHICAL BLOCK menu. A SCHEMATIC VIEW is selected as the IMPLEMENTATION TYPE because we want to draw a schematic for the underlying circuit.

In Figure 4 the REFERENCE has been chosen as CS for Common Source and the IMPLEMENTATION NAME has been chosen to be CS too. I find making them the same makes it easier to keep track of names. Keeping track of names is important when several blocks of the same type are used in the circuit. If the various names are not entered correctly, the block will not be reproduced when you ask for it.

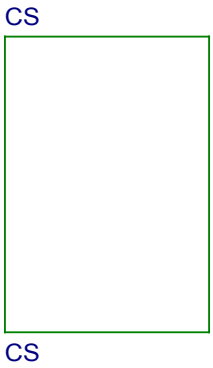

FIGURE 5:
With the mouse, a rectangle of arbitrary size is drawn on the schematic page. The program itself adds the BLOCK REFERENCE and the IMPLEMENTATION NAME at the top and bottom.

Next, hierarchical pins are added, see Figure 6.

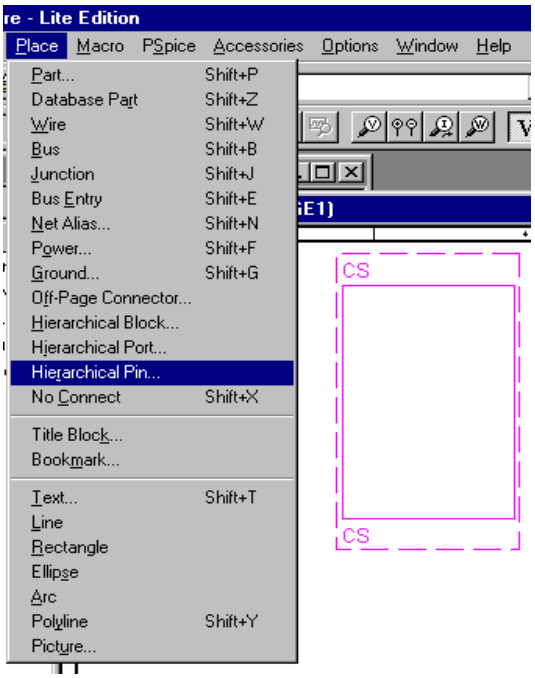

FIGURE 6:
With the block highlighted, selection of PLACE/HIERARCHICAL PIN

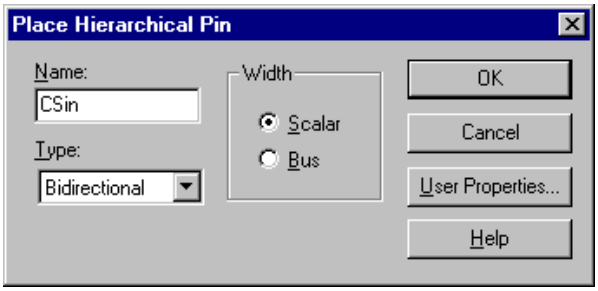

FIGURE 7:
The PLACE HIERARCHICAL PIN menu. The TYPE is immaterial – it just changes the graphic for the pin, but not its function. The NAME is arbitrary as well.

Once the menu of Figure 7 is clicked OK, we can add as many pins as we like all at once, without reactivating the PLACE/HIERARCHICAL PIN menu. They all will have the same name, but their names can be changed later by clicking on them to obtain a PROPERTY EDITOR menu and then changing the NAME property. In this case, I elected to have two supply pins (CSdcP and CSdcN) , one AC input pin (CSin) and one AC output pin (CSout)

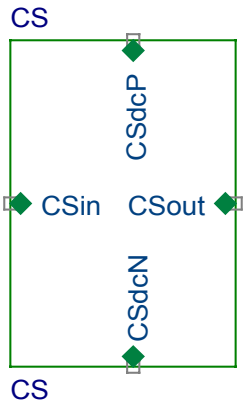

FIGURE 8:
The hierarchical block with the pins added and renamed

At this stage the block is highlighted and the mouse is right-clicked; in the drop-down menu select DESCEND HIERARCHY. A menu appears for naming the schematic.

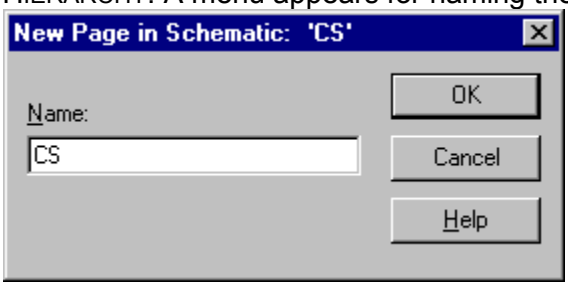

FIGURE 9:
The menu for naming the schematic corresponding to the block.

Again, I choose to name the schematic CS just like the REFERENCE and the IMPLEMENTATION. On clicking OK, a blank SCHEMATIC appears with the connection pins corresponding to the hierarchical block already pasted in. See Figure 10.

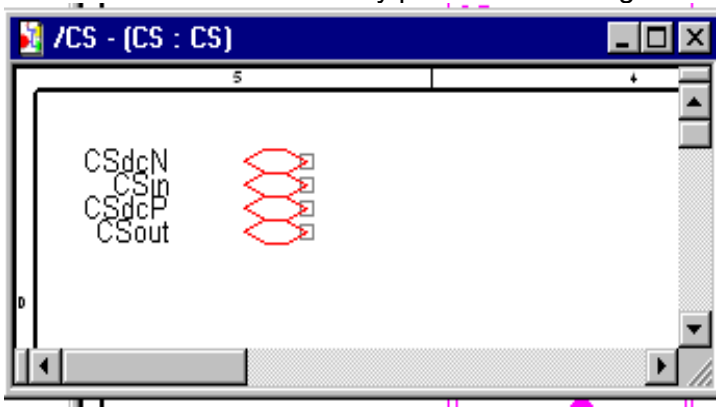

FIGURE 10:
The new schematic obtained by "drilling down" from the hierarchical block

At this point I elect to paste a schematic from another project that includes an already made CS amplifier.

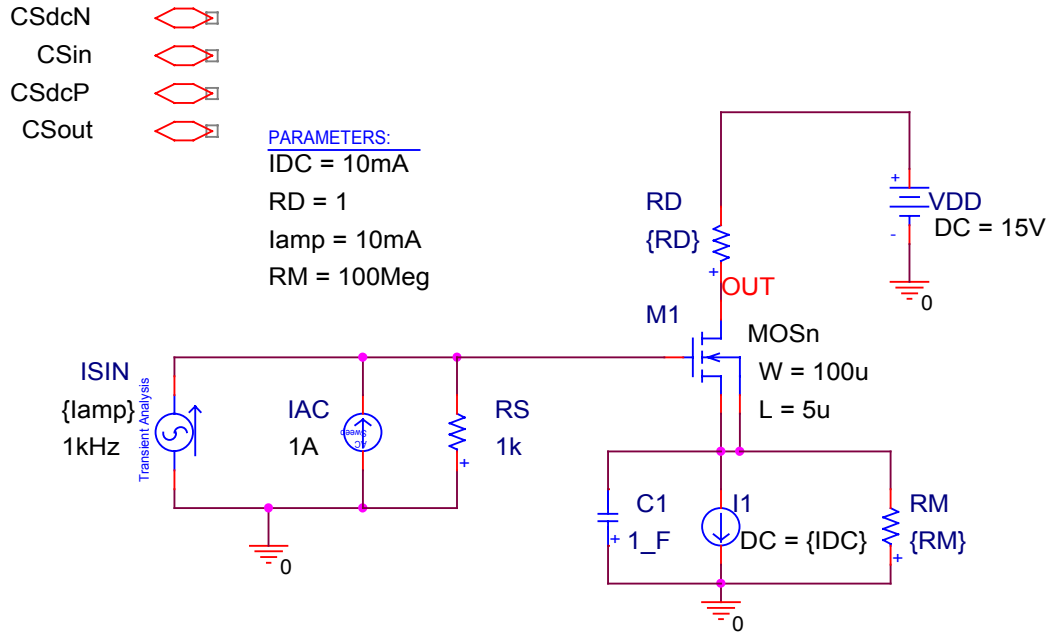

FIGURE 11:

The schematic from another circuit pasted into the block schematic

In Figure 11 there are some modifications to be made. First, the connectors to the world outside the block have to be attached, and the DC sources that are supposed to be outside the block have to be removed. Secondly, the MOSFET is a special part made up from an Mbreakn breakout part. The library for this part has to be added to the MODEL LIBRARY in the •OPJ file.

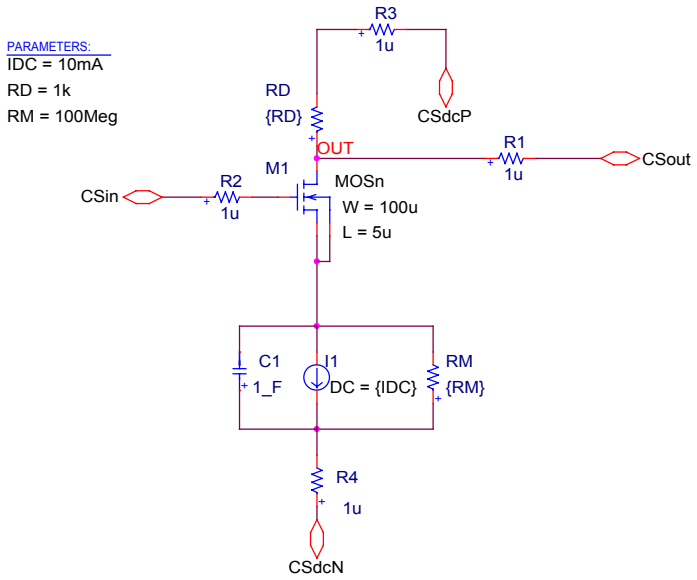

FIGURE 12:

The Common Source Amplifier schematic as modified from Figure 11. The outside world is properly connected to the hierarchical block pins, and parts properly left outside the block are removed..

Figure 12 shows the modified CS amplifier. In each external connection a 1 μΩ resistor has been inserted. These resistors do not change the circuit operation, but they do allow PSPICE to display the currents and voltages at these connections, which can be useful in debugging the circuit. The parameters for the circuit have been placed with the circuit. They could be placed outside the block instead. Which is more useful depends on whether you are interested in the Block view or the Schematic view when you are doing the amplifier design. You cannot have the parameters in both places.

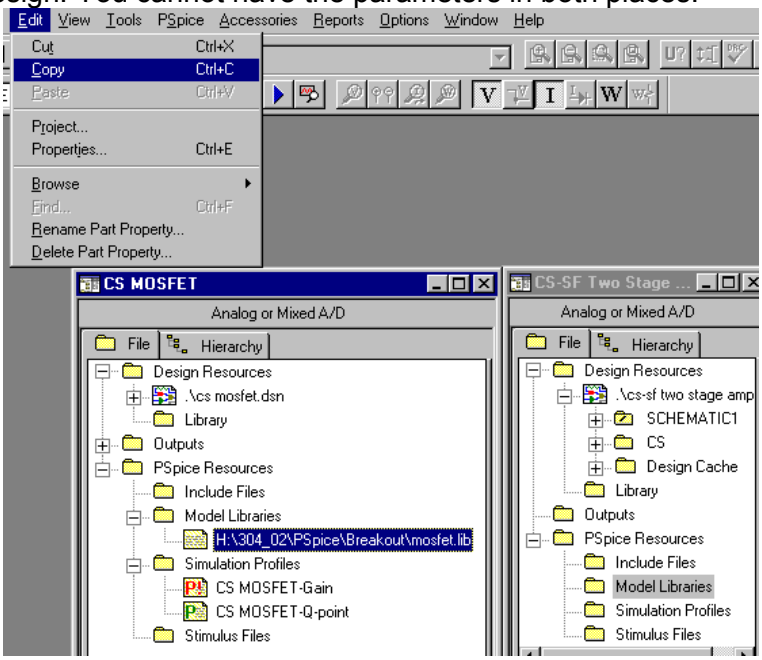

FIGURE 13:

Preparing to copy the file MOSFET.LIB in the CS MOSFET circuit and paste it into the MODEL LIBRARY in the TWO-STAGE AMPLIFIER circuit.

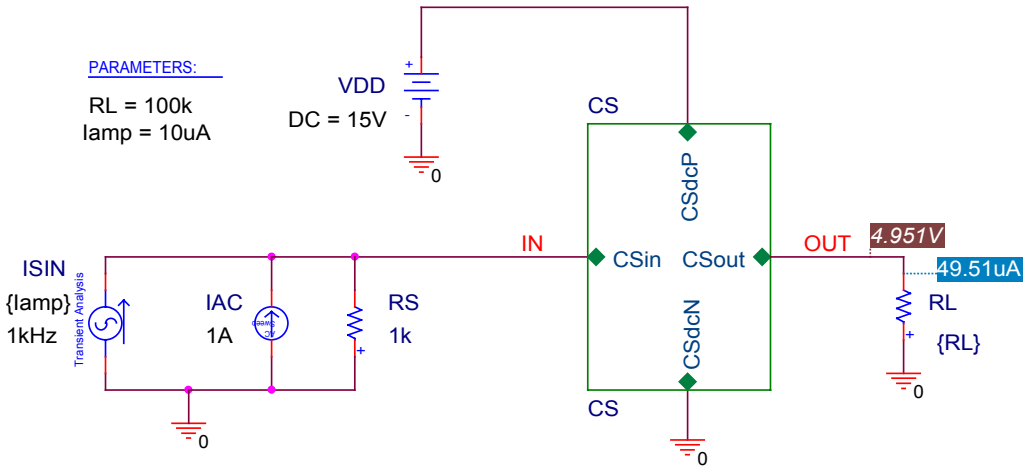

FIGURE 14:

The external connections added to the hierarchical block and a Q-point analysis run

Figure 14 shows the block circuit with the external connections added. A load resistor R_L is attached at the output.

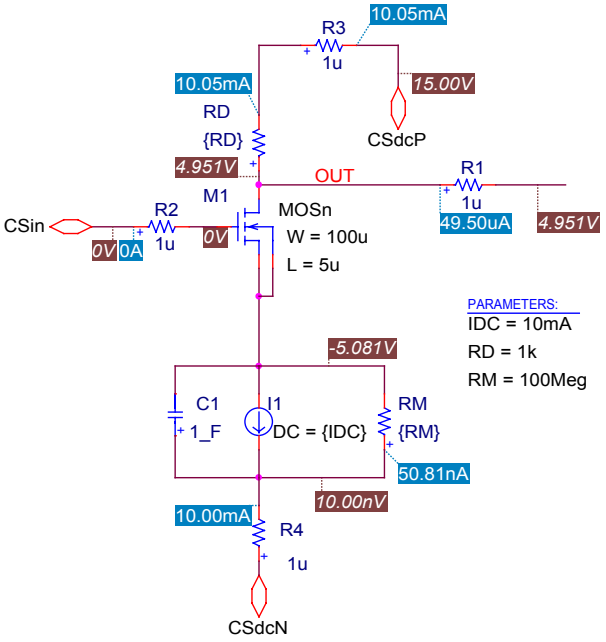

FIGURE 15:

The Q-point data seen at the schematic level when drilling down (descending the hierarchy) from the block of Figure 14.

In Figure 15, because of the 1 μΩ resistors, it is possible to read the currents and voltages at the outside connections. To finish the amplifier, another hierarchical block has to be constructed, called SF for source follower, and the same steps have to be followed. Then the blocks can be connected.

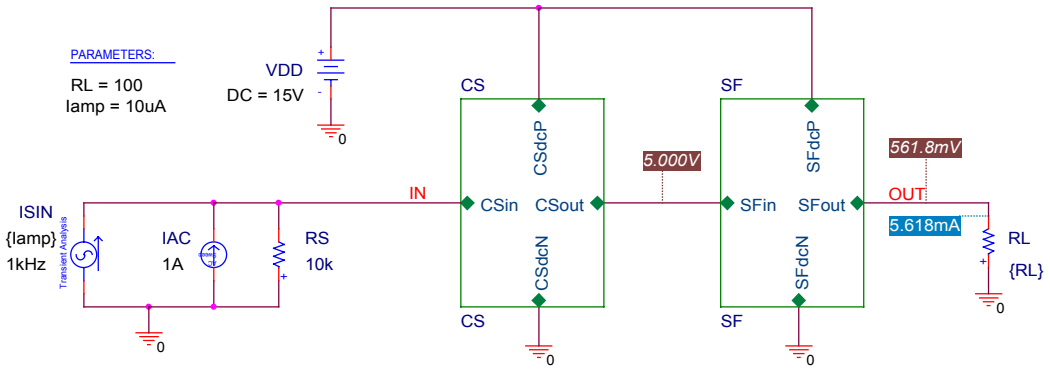

FIGURE 16:

The final block diagram with the source follower added

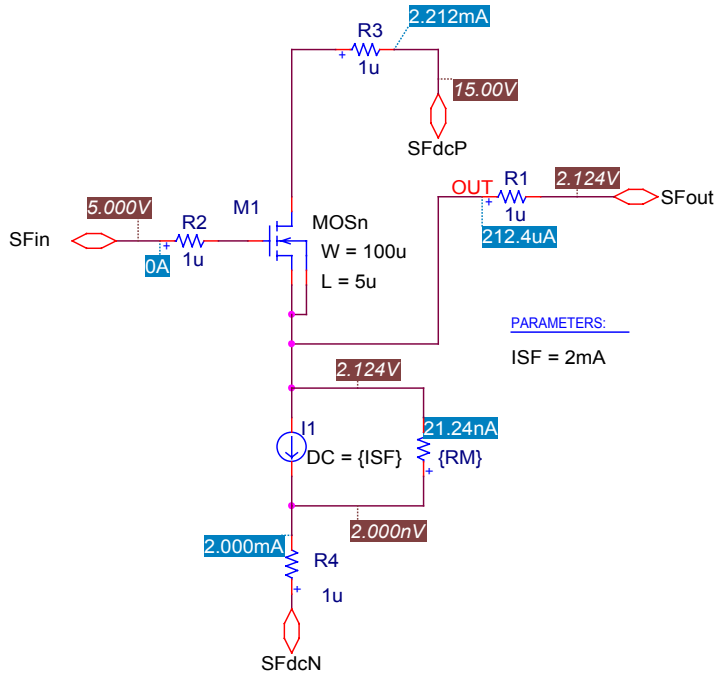

FIGURE 17:

The Source Follower at the Q-point on drilling down from the SF hierarchical block

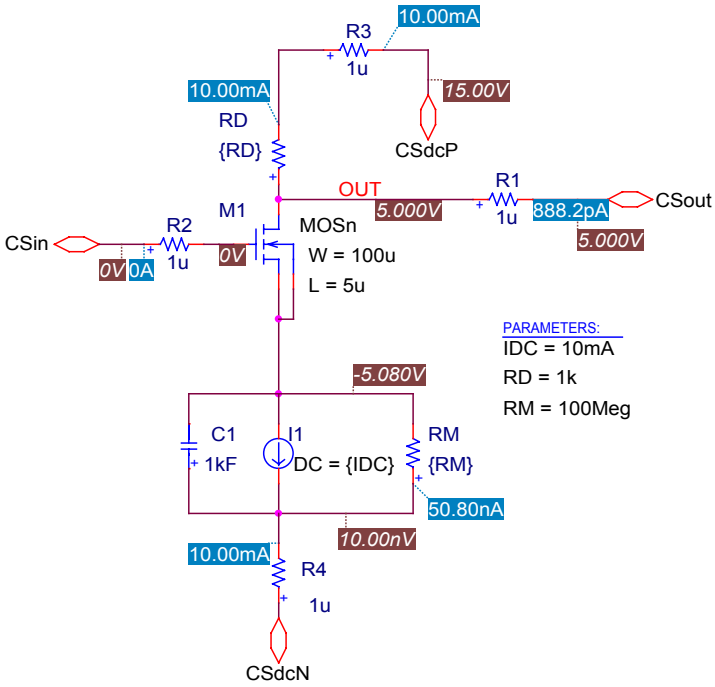

FIGURE 18:

The Common Source amplifier on drilling down from its hierarchical block. The Q-point values in this figure differ from those in Figure 15 because the SF loads the CS differently than the load resistor of Figure 14.