ECE 304: Design of Simplified V_{BE}-Multiplier Output Stage

Schematic

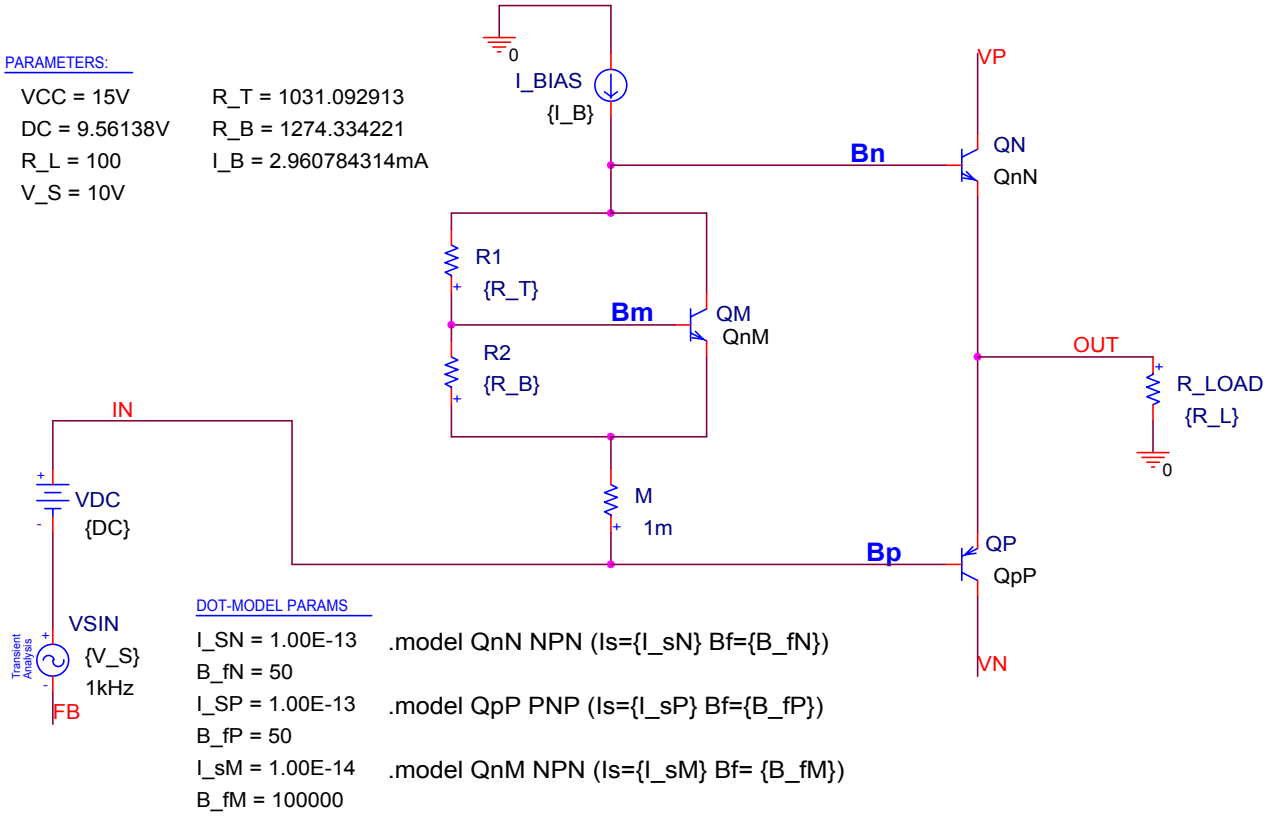


FIGURE 1
A simplified V_{BE}-multiplier output stage

In the schematic of Figure 1, the 1mΩ resistor M is simply a PSPICE convenience used to get PSPICE to monitor the current in the multiplier and label it on the schematic. It doesn't affect the circuit operation, and is not really part of the circuit. The multiplier can use a PNP or an NPN transistor.

Objectives

We will design this stage using this input information: value of load R_L, desired output swing V_O, and desired harmonic distortion.

Simplifications

We use a current source for biasing the stage: in practice this would be a current mirror. The main differences are that the mirror cannot be driven too high or it will saturate, and the mirror has a current that varies with the voltage drop across it. We also assume the β-value for the multiplier is very large, so the multiplier base current doesn't matter.

Design variables

Design variables are variables we introduce to simplify the design or to make it easier to understand. They often are not actual circuit component values, like resistor values, although sometimes they are.

One design variable is the Q-point emitter current of transistor Q_N for V_{OUT} = 0V, namely I_Q. This current is a measure of the crossover distortion, with a larger I_Q implying less crossover distortion. We do not have a simple connection between I_Q and the specified distortion, so we use I_Q in the design and then adjust I_Q using PSPICE to get the crossover distortion we want.

Two other design variables are used, which are related to how we think the circuit works. They are the minimum multiplier current I_M (the smallest current flowing through resistor M), and the smallest collector current flowing through the multiplier transistor I_{CMIN}. The idea behind these two variables is that the multiplier should not be allowed to cut off. Therefore, we need to set the minimum current I_{CMIN} large enough to avoid cutoff. When this current I_{CMIN} flows in the multiplier transistor, the current in the multiplier is larger than I_{CMIN} because of the current in the resistor divider made up of R_T and R_B. We set the minimum multiplier current at I_M to avoid starving the base current of the multiplier transistor. These two currents are not known in advance, so they are adjustable parameters of the design that can be tweaked to obtain good performance.

Among other things, we want to insure that the gain of the stage is nearly one for the entire range of output voltages, and that involves (i) keeping the resistance of the multiplier low, and (ii) keeping the stage linear, which is hardest to achieve for large voltages. The harmonic distortion will be caused by a combination of crossover distortion and the distortion due to this nonlinearity. For the moment, we imagine that the choice of I_{CMIN} and I_M might affect these two performance characteristics. As with I_Q, we will find from PSPICE just what their effects are.

Analysis

The analysis is based on two bias conditions, the high output voltage condition when $\upsilon_{OUT} = V_O$, the maximum output swing, and the Q-point where the output voltage $\upsilon_O = 0V$. Each condition allows part of the design to be found.

High output voltage

This bias condition tells us the correct values for I_B and R_B.

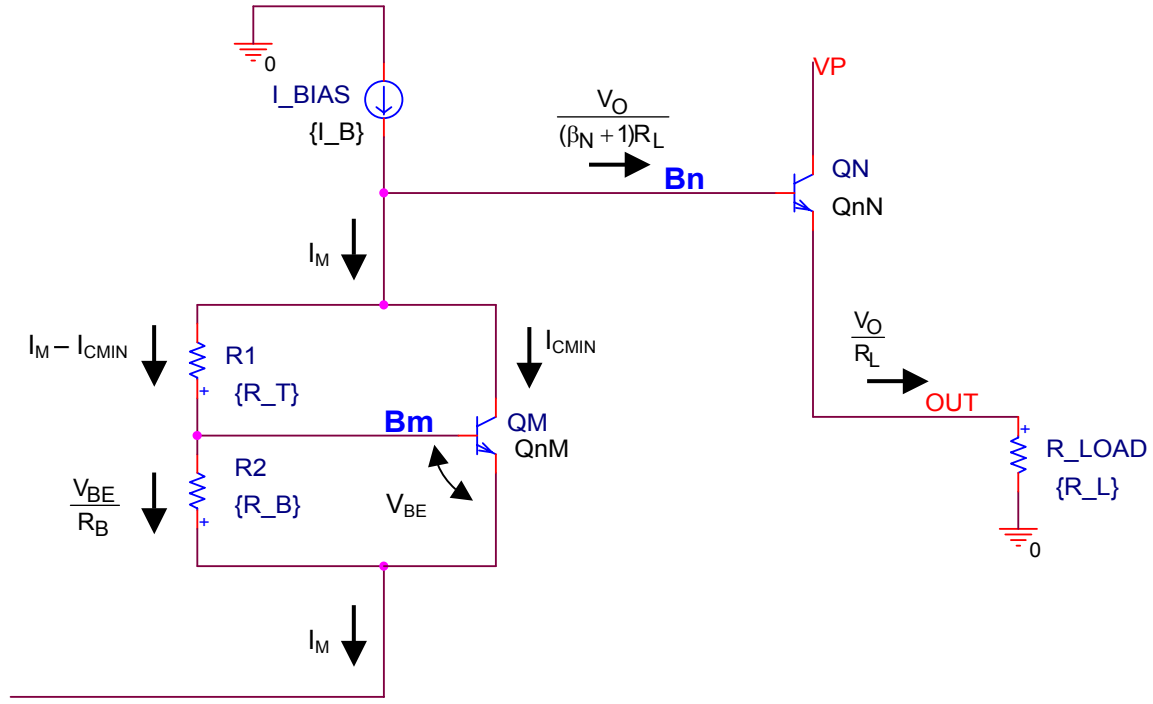


FIGURE 2

High output voltage case with output voltage $\upsilon_O = V_O$, the maximum output voltage

In the high output voltage case, the PNP is cutoff, so the circuit is as Figure 2. KCL at the base node of QN determines the bias current I_B:

EQ. 1

$$I_B = I_M + \frac{V_O}{(\beta_N + 1)R_L}.$$

The diode law determines V_{BE}:

EQ. 2

$$V_{BE} = V_{TH}\ell n\,(I_{CMIN}/I_{sM}).$$

If we neglect the base current in the multiplier, the current in R_B is $I_M - I_{CMIN}$. Then Ohm's law determines R_B:

EQ. 3

$$R_B = \frac{V_{BE}}{I_M - I_{CMIN}}.$$

As pointed out earlier, I_M and I_{CMIN} are introduced as design variables: that is, we set up the design as though I_M and I_{CMIN} are known, set up a spreadsheet as a function of these variables, and then choose their values from plots on the spreadsheet to optimize the specs.

Zero output voltage case

This bias condition tells us the correct value of R_T.

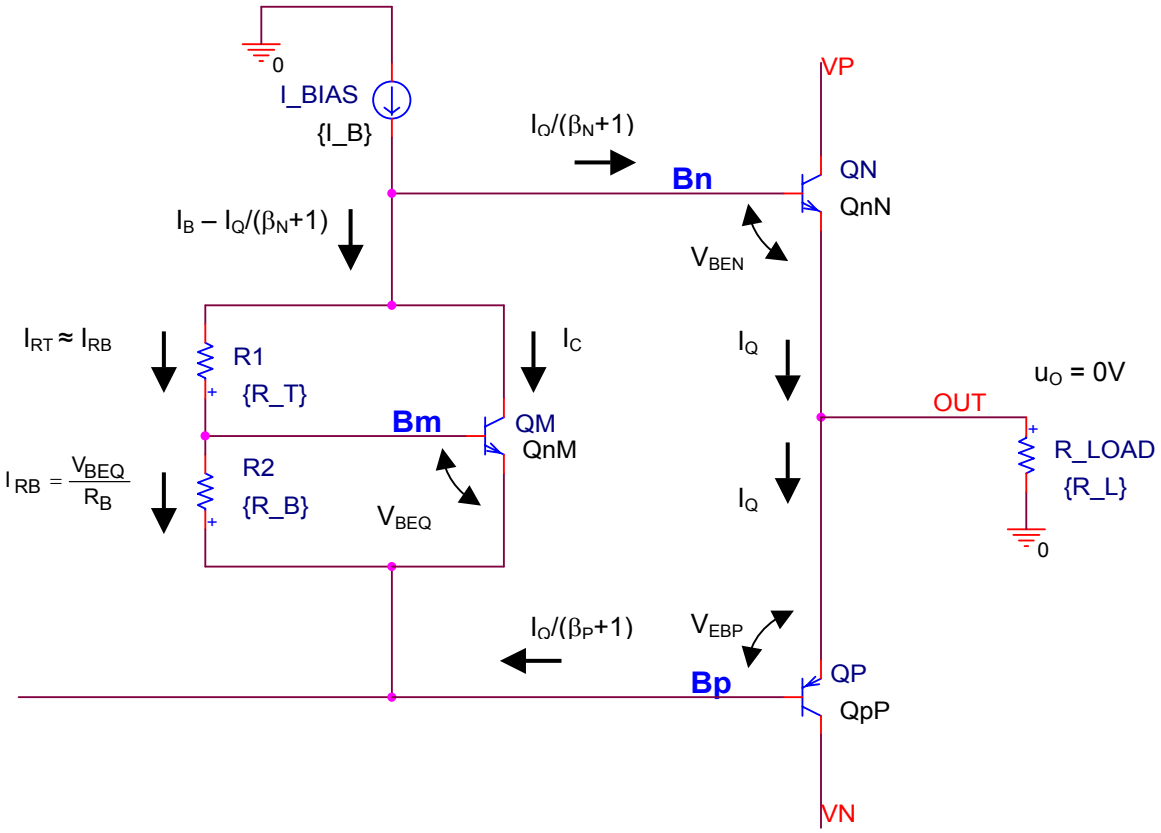


FIGURE 3

The setup for zero output voltage

The voltage across the entire multiplier is the base-to-base voltage V_{BB} given by

EQ. 4

$$V_{BB} = V_{BEN} + V_{EBP}.$$

It is this voltage V_{BB} that decides the amount of crossover distortion, and the voltages in EQ. 4 are found from the diode law and the specified I_Q as

EQ. 5

$$V_{BEN} = V_{TH}\ell n\left(\frac{\beta_N}{\beta_N + 1}\bullet\frac{I_Q}{I_{sN}}\right) \qquad V_{EBP} = V_{TH}\ell n\left(\frac{\beta_P}{\beta_P + 1}\bullet\frac{I_Q}{I_{sP}}\right).$$

With EQ. 4 and EQ. 5 V_{BB} is known.

We design the multiplier to produce the voltage V_{BB} of EQ. 4. This voltage is set by the sum of the voltage drops across the resistors R_T and R_B. The drop across R_B is the base-emitter voltage V_{BEQ} of the multiplier transistor. We have to find this voltage. We begin with the diode law, which gives the base-emitter voltage in the multiplier as:

EQ. 6

$$V_{BEQ} = V_{TH}\ell n\ (I_C/I_{sM}).$$

To use EQ. 6, we need the collector current I_C. To find I_C, we find the current in the resistor branch and apply KCL to the node at the top of the multiplier. First, Ohm's law and V_{BEQ} determine the current in R_B as:

EQ. 7

$$I_{RB} = V_{EBQ}/R_B.$$

Neglecting base current to the multiplier transistor, $I_{RB} \approx I_{RT}$. We then know the current I_C in the multiplier transistor using KCL at the collector:

EQ. 8

$$I_C = I_B - \frac{I_Q}{\beta_N + 1} - I_{RT} \approx I_B - \frac{I_Q}{\beta_N + 1} - \frac{V_{BE}}{R_B}.$$

We plug EQ. 8 into EQ. 6 to find V_{BEQ}:

EQ. 9

$$V_{BEQ} = V_{TH}\ell n\left(\frac{I_B - I_Q/(\beta_N + 1) - V_{BEQ}/R_B}{I_{sM}}\right).$$

EQ. 9 is solved by iteration beginning with substitution on the right side using $V_{BEQ} \approx 0.7$ V, evaluating EQ. 9 for a new V_{BEQ}, substituting the new value on the right, and so forth. We now know V_{BEQ}, and the current $I_{RB} = V_{BEQ}/R_B \approx I_{RT}$. The total drop across the multiplier is

EQ. 10

$$V_{BB} = I_{RT}R_T + I_{RB}R_B \approx (R_T + R_B)\ V_{BEQ}/R_B = (1+R_T/R_B)\ V_{BEQ}.$$

EQ. 10 is the reason the circuit is called the V_{BE}-multiplier, namely, the voltage drop across it multiplies V_{BE} by the factor $(1+R_T/R_B)$. Using the known value of V_{BB} from EQ. 4 in EQ. 10, we find the necessary value of R_T as shown in EQ. 11 below

EQ. 11

$$R_T = \left(\frac{V_{BB}}{V_{BEQ}} - 1\right)R_B.$$

The design is now complete, with R_T from EQ. 11, R_B from EQ. 3, and I_B from EQ. 1.

Summary

The input data includes the dot-model parameters of the transistors, the maximum output swing voltage V_O, the minimum load resistance R_L, and the maximum allowed harmonic distortion.

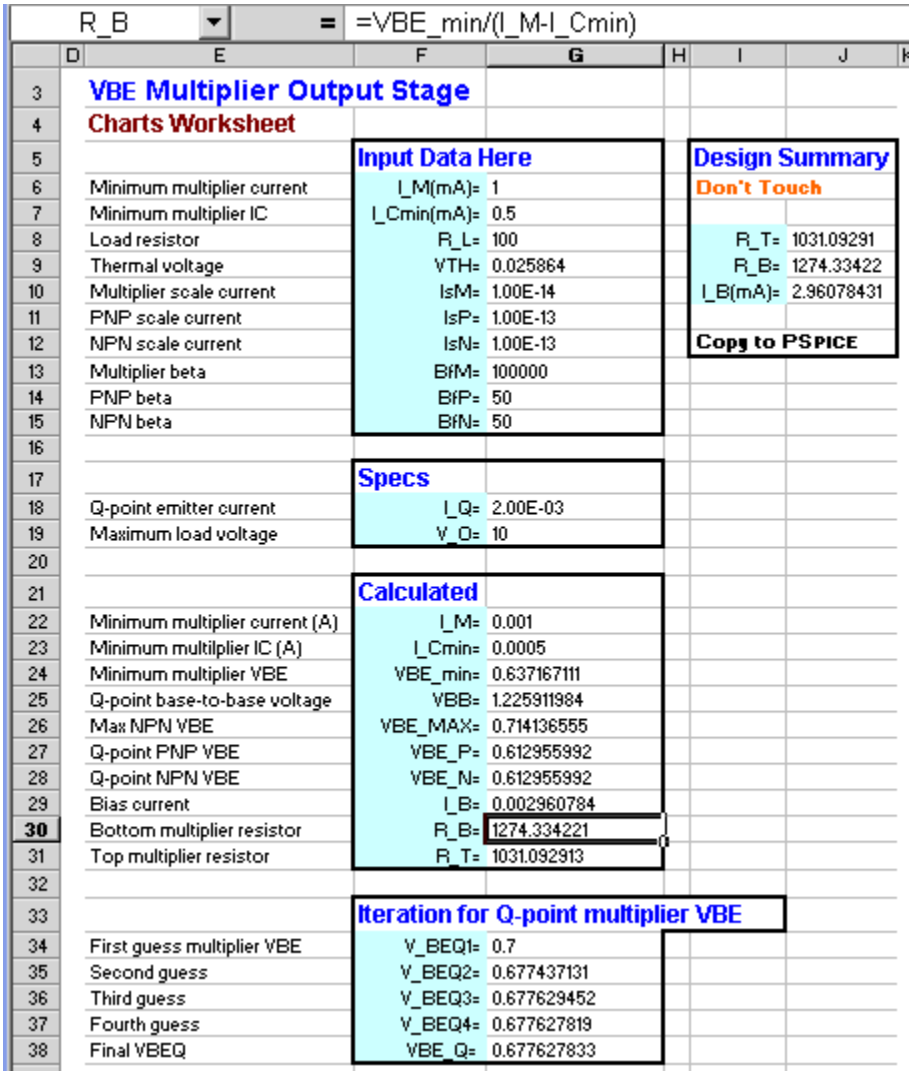
The design is based upon three design variables, the Q-point current I_Q in the output transistors at zero output voltage, the minimum multiplier current I_M, and the minimum multiplier transistor's collector current I_{CMIN}.

Current I_Q controls distortion due to crossover, which can be estimated using Fourier analysis of a TRANSIENT simulation profile in PSPICE.

The two minimum currents I_M and I_{CM} flow in the *high* voltage output case, because it is in the high voltage case that the base current to the output transistor is high. They are specified to avoid cutoff of the multiplier transistor in this worst-case situation, and have some influence on the amplifier gain and linearity.

PSPICE verification of analysis

Spreadsheet



R_B = =VBE_min/(I_M-I_Cmin)

	E	F	G	I	J
3	VBE Multiplier Output Stage				
4	Charts Worksheet				
5		Input Data Here		Design Summary	
6	Minimum multiplier current	I_M(mA)=	1	Don't Touch	
7	Minimum multiplier IC	I_Cmin(mA)=	0.5		
8	Load resistor	R_L=	100	R_T=	1031.09291
9	Thermal voltage	VTH=	0.025864	R_B=	1274.33422
10	Multiplier scale current	IsM=	1.00E-14	I_B(mA)=	2.96078431
11	PNP scale current	IsP=	1.00E-13		
12	NPN scale current	IsN=	1.00E-13	Copy to PSPICE	
13	Multiplier beta	BfM=	100000		
14	PNP beta	BfP=	50		
15	NPN beta	BfN=	50		
16					
17		Specs			
18	Q-point emitter current	I_Q=	2.00E-03		
19	Maximum load voltage	V_O=	10		
20					
21		Calculated			
22	Minimum multiplier current (A)	I_M=	0.001		
23	Minimum multilplier IC (A)	I_Cmin=	0.0005		
24	Minimum multiplier VBE	VBE_min=	0.637167111		
25	Q-point base-to-base voltage	VBB=	1.225911984		
26	Max NPN VBE	VBE_MAX=	0.714136555		
27	Q-point PNP VBE	VBE_P=	0.612955992		
28	Q-point NPN VBE	VBE_N=	0.612955992		
29	Bias current	I_B=	0.002960784		
30	Bottom multiplier resistor	R_B=	1274.334221		
31	Top multiplier resistor	R_T=	1031.092913		
32					
33		Iteration for Q-point multiplier VBE			
34	First guess multiplier VBE	V_BEQ1=	0.7		
35	Second guess	V_BEQ2=	0.677437131		
36	Third guess	V_BEQ3=	0.677629452		
37	Fourth guess	V_BEQ4=	0.677627819		
38	Final VBEQ	VBE_Q=	0.677627833		

FIGURE 4
Spreadsheet implementing the analysis above

Figure 1 shows a straightforward implementation of the analysis on a spreadsheet

PSPICE evaluation

We look at the two bias conditions used in the analysis, zero output voltage and high output voltage.

ZERO OUTPUT VOLTAGE

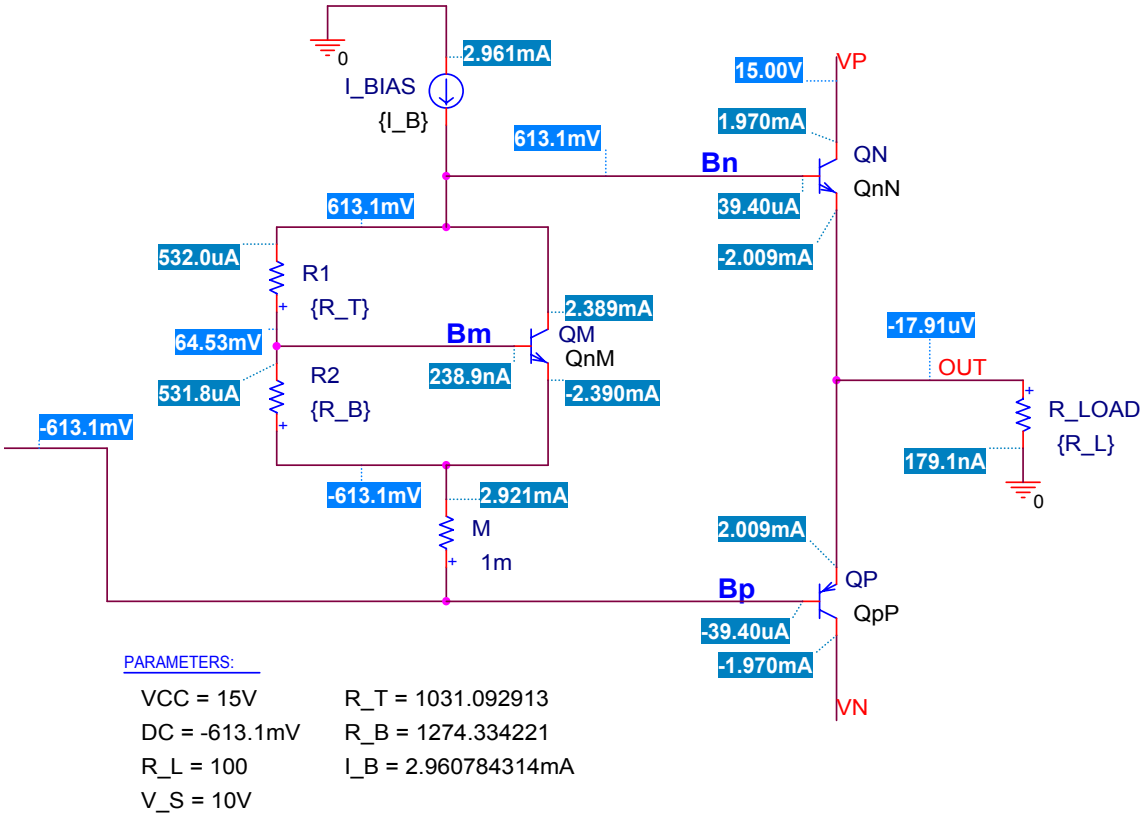


FIGURE 5

Zero-output case; I_Q agrees with spreadsheet

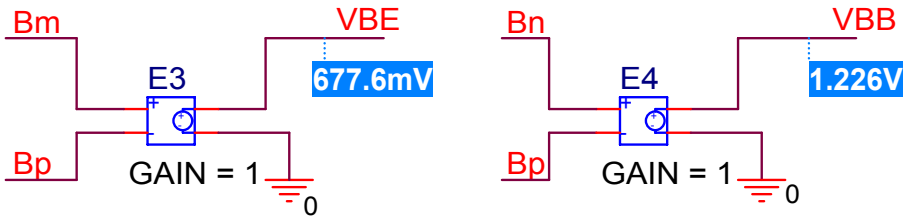


FIGURE 6

PSPICE values for V_{BE} and V_{BB} at the zero-output case; results agree with spreadsheet

Figure 5 and Figure 6 show the spreadsheet agrees with PSPICE at zero volts output. The values of I_Q, V_{BB} and V_{BE} agree with the spreadsheet.

HIGH OUTPUT VOLTAGE

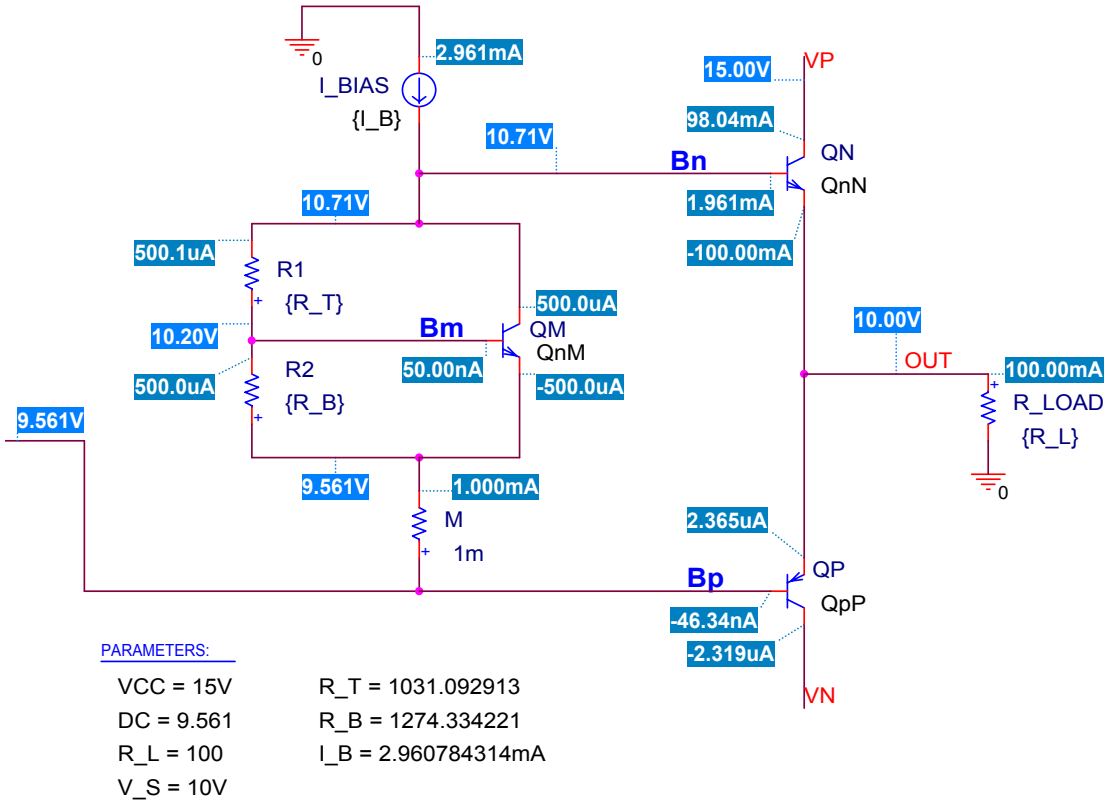


FIGURE 7

High voltage output case υ_O = 10V; PSPICE currents in multiplier agree with spreadsheet;

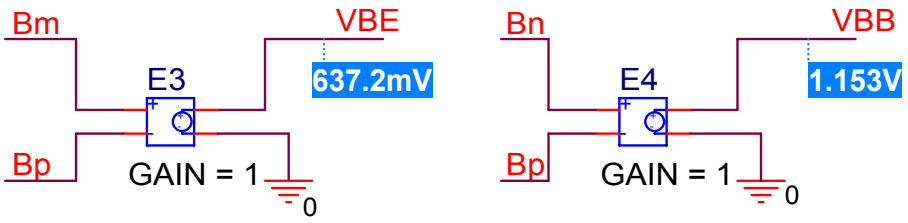


FIGURE 8

PSPICE value multiplier V_{BE} (VBE_min) at the maximum-output case; result agrees with spreadsheet; V_{BB} at high output is not calculated explicitly on the spreadsheet

Figure 7 and Figure 8 show PSPICE agrees with the spreadsheet at υ_O = 10V. Although a current of 2.4 μA in Q_P is not really cut off, it is far too low compared to the current in Q_N to affect the analysis, so it might as well be cut off. We conclude that the analysis is correct, within its assumptions.

Distortion evaluation

Having a design, the next step is to compare it with the specifications. We already see that it comes close to driving the output up to 10V and has the selected value of I_Q when the output is zero. The next question is whether we actually chose good values for I_Q, I_M and I_{CMIN}.

We do a transient analysis and a gain plot to look at the distortion. If we have an actual number for the harmonic distortion we want, from these plots we can assess whether the amplifier has low enough distortion. If it does not, we can try adjusting I_Q, I_M and I_{CMIN} to get the best results possible. We may find we have a trade-off situation, where improving one performance goal makes another one worse. If we cannot get the results we want, we will have to use a different circuit.

For sure we will have the trade-off of lower power efficiency for better crossover distortion, as this trade-off is built into the Class AB amplifier.

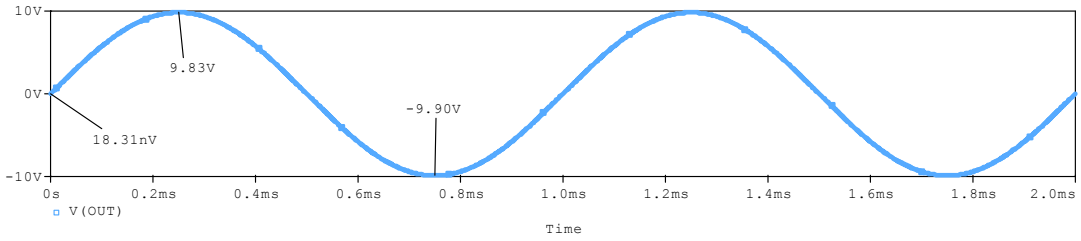


FIGURE 9

Transient output for 10V sinusoidal input

Figure 9 shows we have a pretty good sinusoidal output, although there is some asymmetry because the upswing and downswing aren't quite the same (nonlinearity). A more quantitative estimate of distortion comes from the Fourier analysis feature of PSPICE.

HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.00E+03	9.85E+00	1.00E+00	8.40E-07	0.00E+00
2	2.00E+03	1.63E-02	1.65E-03	9.00E+01	9.00E+01
3	3.00E+03	2.04E-02	2.07E-03	-1.80E+02	-1.80E+02
4	4.00E+03	2.25E-04	2.29E-05	9.00E+01	9.00E+01
5	5.00E+03	1.16E-02	1.17E-03	-1.80E+02	-1.80E+02
6	6.00E+03	8.01E-04	8.13E-05	9.00E+01	9.00E+01
7	7.00E+03	6.37E-03	6.47E-04	-1.80E+02	-1.80E+02
8	8.00E+03	3.19E-04	3.24E-05	9.00E+01	9.00E+01
9	9.00E+03	4.18E-03	4.25E-04	-1.80E+02	-1.80E+02
10	1.00E+04	2.22E-04	2.25E-05	9.00E+01	9.00E+01
11	1.10E+04	2.89E-03	2.93E-04	-1.80E+02	-1.80E+02
12	1.20E+04	1.46E-04	1.48E-05	9.00E+01	9.00E+01
TOTAL HARMONIC DISTORTION = 3.014943E-01 PERCENT					

FIGURE 10

PSPICE harmonic distortion from PROBE output file is ≈ 0.3%

A very visual idea of the distortion comes from a gain plot, as shown in Figure 11. Figure 11 has a pronounced dip in the center, which is the crossover region. It also sags at high voltages, which is nonlinearity not related to crossover distortion. We see that using lower amplitude, say 8V instead of 10V, will help because the sag at high voltages will not play a part. To get better linearity, maybe we could just design the amplifier for a design V_O that is larger than the 10V we are really going to use?

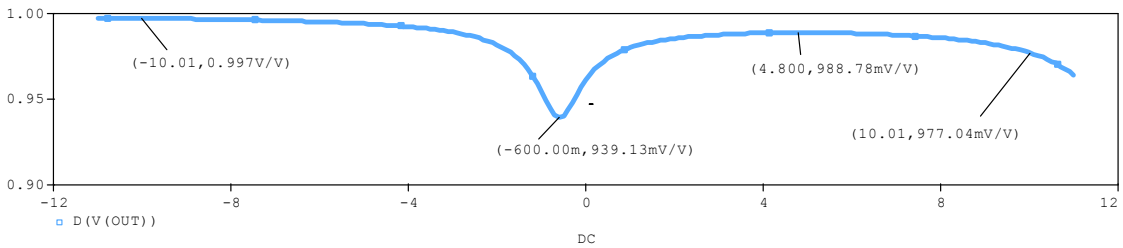


FIGURE 11

Gain plot for amplifier; crossover distortion results from the dip in the middle of the gain curve; additional distortion is present because of fall-off at large output voltages

We also could look at a few different values of the design parameters I_Q, I_M and I_{CMIN} to get an idea of just what they do to the distortion.

Power efficiency evaluation

Using PSPICE we can find the power efficiency of the amplifier. In PROBE we run a TRANSIENT simulation profile. Then we use the PSPICE function S() to integrate the current-voltage products for the load (useful power), the two power supplies and the current bias.

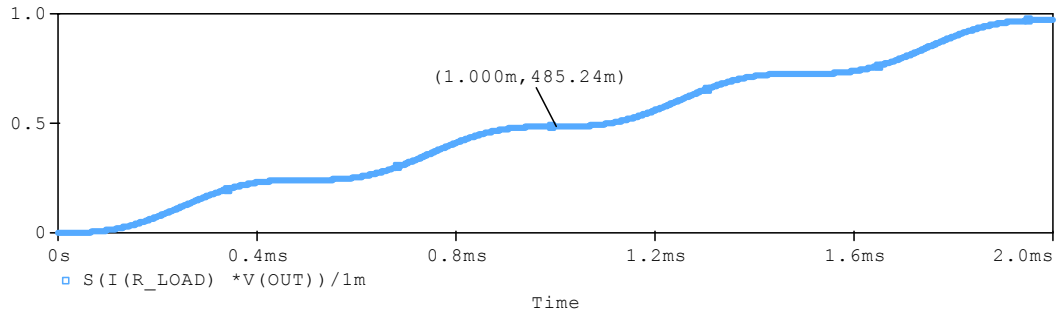


FIGURE 12

PSPICE integration of *I-V* product for the load; average power = 485.2 mW

Figure 12 shows the integrated *I-V* product for the load vs. time t, which is the total power consumed by the load up to time t. This power is divided by the period of the waveform T=1ms, so the average power over one period is the value of this curve at time t =1ms.

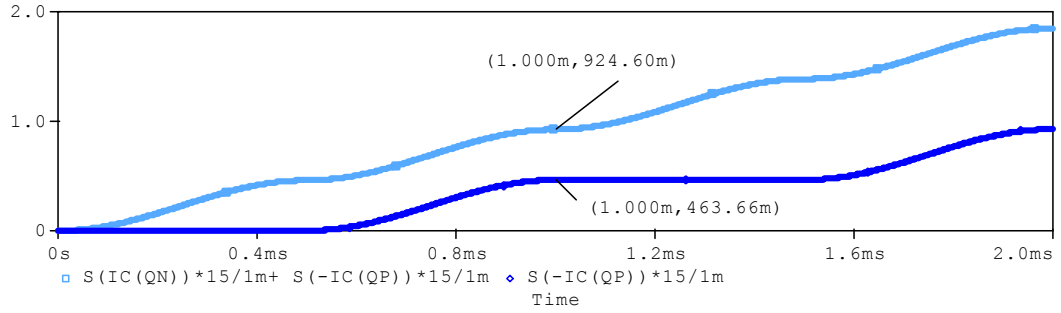


FIGURE 13

Integrated *I-V* product for the two power supplies: top curve is sum of power for both supplies showing average power of 924.6 mW, bottom curve is the power delivered by the negative power supply alone

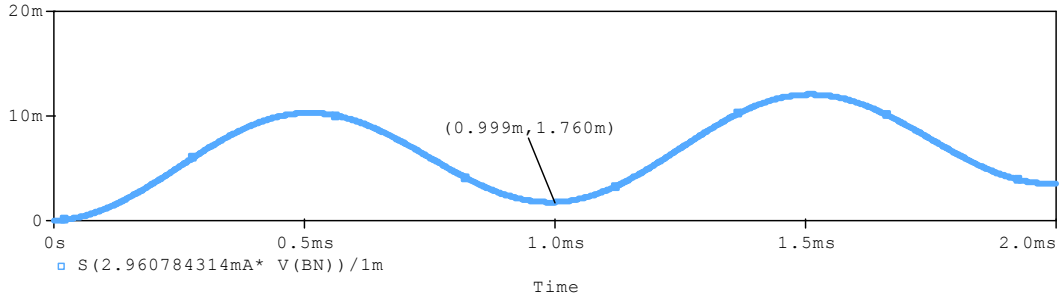


FIGURE 14

Power delivered by current source I_B showing average power of 1.8 mW

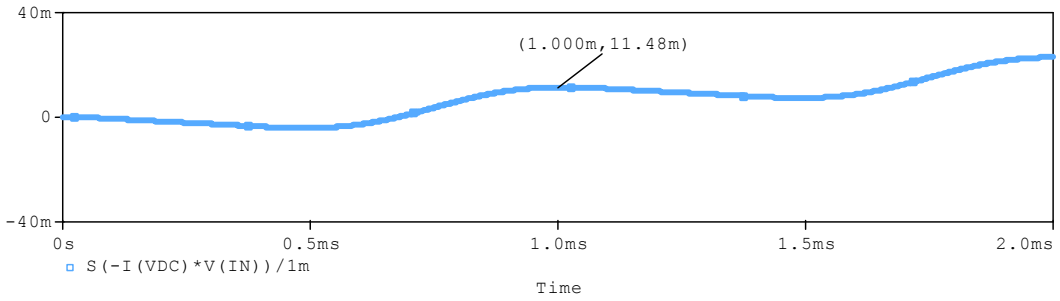


FIGURE 15
Power input by signal source of 11.5mW

The power efficiency is then

EQ. 12

$$\eta = \frac{\text{Useful power to load}}{\text{Power input}} = \frac{485.2\text{mW}}{1.8\text{mW} + 11.5\text{mW} + 924.6\text{mW}} = 52\% \ .$$

Neither the power contributed by the signal source nor the DC bias source is large enough to affect the power efficiency, at least in this case.

Exercises

1. Extend the analysis to include the base current of the multiplier transistor.
2. Extend the analysis to include the Early voltage of the multiplier.
3. Extend the analysis to include different values for β at different current levels; for example, β_N of the NPN is different for high currents than for low currents.
4. Extend the analysis to include a current mirror to supply the bias current, and take into account that the mirror supplies a different current at the Q-point than for maximum output voltage. That is, take the mirror resistance into account.
5. Do a small-signal analysis for both a high and low DC output voltage to see how close the gain is to one, to check the distortion due to gain variation, and to see how the resistance of the multiplier circuit affects the gain.
6. Extend the analysis to include a voltage follower input stage. In this case the downswing analysis is necessary to design the voltage follower so it will not cut off.
7. Make a spreadsheet for each of the above extensions.