ECE 304 Spring '06 Exam 2 Solutions

For all problems take the thermal voltage as V_{TH} = 25.864 mV.

Problem 1: Operational amplifier design

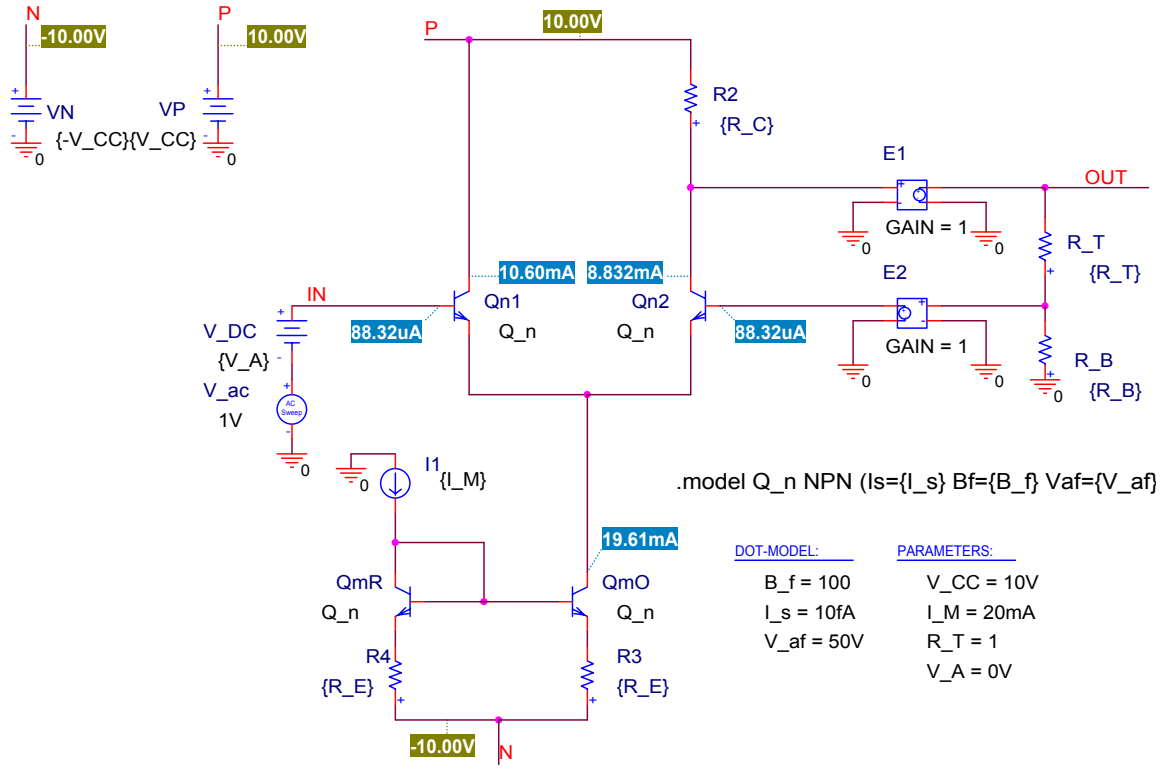


FIGURE 1

Operational amplifier for Problem 1 for input voltage V_A = 0 V

The amplifier of Figure 1 is intended for use as a noninverting operational amplifier.

1. The VCVS part E1 could be called an ideal voltage follower. What is its function in the circuit? Why not leave it out?

Answer: E1 presents an open circuit to the collector of Qn2. Consequently, (i) there is no current drawn to the feedback network to disturb the Q-point of the amplifier and (ii) the feedback network does not shunt R_C so the feedback network does not disturb the gain of the amplifier.

2. What is the role of the VCVS part E2? Why not leave it out?

Answer: E2 presents an open circuit to the center node of the feedback network. Consequently, there is no current drawn from this center node, and the feedback network is a perfect voltage divider. Secondly, E2 provides base current directly to Qn2, just like the input side. So E2 supplies base current in a symmetrical way that does not contribute to imbalance of the amplifier, unlike the case of base current supplied through a resistor, for example, through R_B and R_T..

3. Will the circuit work the same way for any choice of values for R_T and R_B, as long as the ratio R_T/R_B has the correct value? Explain.

Answer: The differential amplifier senses only the voltage at the center of the feedback divider, and as this voltage depends only on the ratio R_T/R_B, the amplifier is insensitive to the absolute values of R_T and R_B.

4. Select values for R_C, R_B, and R_E so the differential amplifier will have a gain of approximately 2 V/V for 0 V ≤ V_A ≤ 5 V, assuming zero tolerance of forward bias of the CB junctions: V_{sat} = 0 V. The resistor R_C is chosen for maximum differential voltage gain compatible with this transfer curve. Likewise, the mirror leg resistors are chosen to have the largest compatible values of R_E. Show your work in your outline.

Answer: $R_T = R_B$ = 1 Ω, R_C = 1132.4 Ω, R_E = 432.0 Ω.

Outline: The collector current in Figure 1 is related to the base current by EQ. 1 below.

EQ. 1

$$\beta = \frac{I_C}{I_B} = \frac{8.832\ \text{mA}}{88.32\ \mu\text{A}} = 100 \ = \text{Bf}.$$

Because $\beta = Bf(1+V_{CB}/V_{af})$, EQ. 1 shows that $V_{CB} = 0$ V in Figure 1. That means in turn that there is no current drawn in the feedback network and the base voltage of Q2n is zero. Consequently, R_C has a drop of 10 V across it, and Ohm's law provides R_C as

EQ. 2

$$R_C = \frac{10\,\text{V}}{8.832\,\text{mA}} = 1132.4\,\Omega\ .$$

At this bias condition the emitter of the differential amplifier is at its lowest value for $0 \le V_A \le 5$ V. The largest compatible value of R_E will bring the base voltage of the mirror V_B to equal this emitter voltage of the DA, V_E. The base voltage of the mirror is

EQ. 3

$$V_B = -V_{CC} + I_E R_E + V_{BE}(\text{QmO}) = V_E = -V_{BE}(\text{Q2n})\ .$$

We now evaluate these terms.
The current in the collector of the mirror is $I_M = 19.61$ mA.
When the base of the mirror is at the emitter voltage of the DA, V_{CB} of the mirror output transistor is zero. Therefore, its β also is β = Bf. Therefore, the leg current in the mirror is

EQ. 4

$$I_E = (1 + 1/\beta)\ I_M \ = 1.01 \times 19.61\ \text{mA} = 19.806\ \text{mA}.$$

Because V_{CB} of the mirror transistor QmO is zero, V_{BE} is given by

EQ. 5

$$V_{BE}(\text{QmO}) = V_{TH} \ln\left(\frac{I_M}{I_S}\right) = 25.864\text{mV} \ln\left(\frac{19.61\text{m}}{10\text{fA}}\right) = 732.07\ \text{mV}.$$

Likewise, the V_{BE} of the DA transistor Qn2 is

EQ. 6

$$V_{BE}(\text{Q2n}) = V_{TH} \ln\left(\frac{I_C}{I_S}\right) = 25.864\text{mV} \ln\left(\frac{8.832\text{m}}{10\text{fA}}\right) = 711.44\ \text{mV}.$$

Consequently, we find R_E from EQ. 3 as

EQ. 7

$$R_E = \frac{V_{CC} - V_{BE}(\text{QmO}) - V_{BE}(\text{Q2n})}{I_E} = \frac{10 - 732.07\text{m} - 711.44\text{m}}{19.806\text{m}} = 432.0\ \Omega.$$

The circuit depends only on the ratio of R_T/R_B. The gain with feedback is ideally $A_{fb} = 1 + R_T/R_B = 2$ V/V, so $R_T = R_B$. The value of R_T is given as $R_T = 1\ \Omega$, so $R_B = 1\ \Omega$.

5. For an input voltage of $V_A = 8$ V, tabulate the modes of all transistors. Explain your table in your outline.

Answer:

V_A=8 V	
Transistor	Mode
Qn1	A
Qn2	CO
QmR	A
QmO	A

Outline: As V_A increases to $V_A = 5$ V, the collector voltage of Qn2 increases toward 10V, and the voltage drop across its R_C tends to zero. Therefore, the current in Qn1 increases toward the mirror current, while Qn2 tends toward cutoff. For Qn1, $V_{CB} = 2$ V, so Qn1 remains active. The emitter voltage of the DA will be V_{BE} below 8V, so the mirror will be well above its compliance voltage and all mirror transistors are active.

6. For an input voltage of $V_A = -5$ V, tabulate the modes of all transistors. Explain your table in your outline.

Answer:

V_A = -5 V	
Transistor	Mode
Qn1	CO
Qn2	SAT
QmR	A
QmO	SAT

Outline: At V_A = 0V, Qn2 already is on the edge of saturation. As V_A is made negative, Qn2 saturates. The base voltage of Qn2 cannot change much once Qn2 saturates, locking the emitter voltage of Qn2 at V_{BE} lower than this. (To be more precise, the drop across R_T is $-V_{SAT}$, so the drop across R_B is also $-V_{SAT}$, and the base of Qn2 is at $-V_{SAT}$.) Transistor Qn1 has the same emitter voltage, which therefore also is fixed and, as V_A is made more negative, Qn1 is driven to cutoff. In addition, Qn2 draws a large base current, which adds to its emitter current and must be drawn by the mirror. Thus, Qn1 also tends to cut off because the mirror has only enough current to handle the saturated Qn2. In the mirror, QmO is saturated and QmR remains active as its V_{CB} = 0 V.

7. For an input voltage of V_A = 2.5 V, tabulate the modes of all transistors. Explain your table in your outline.

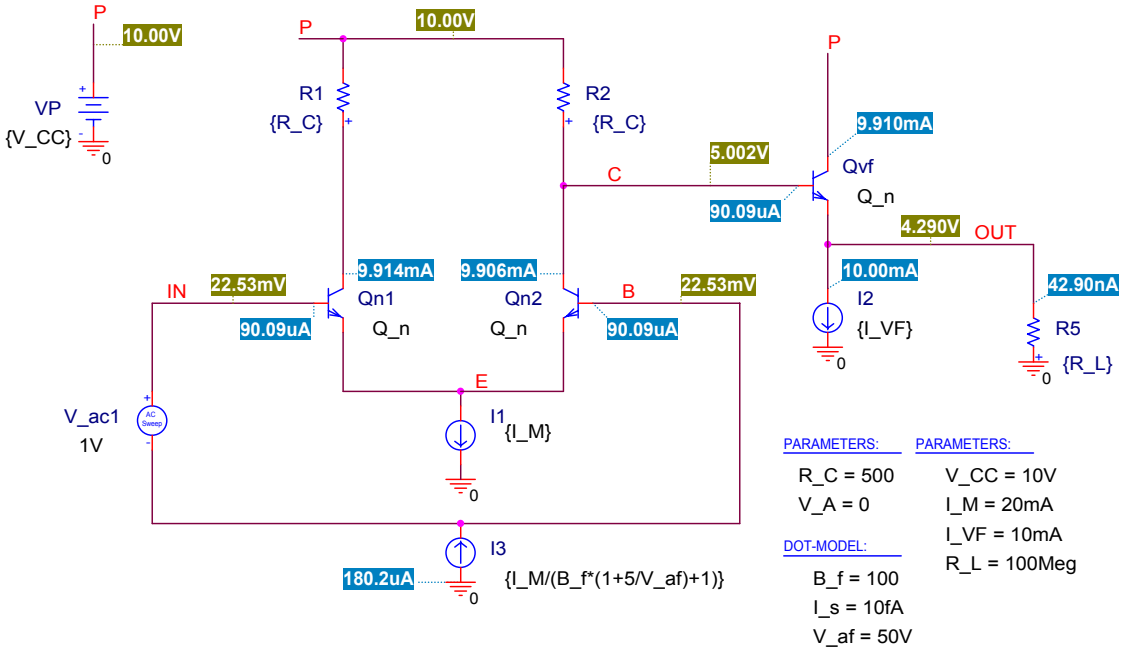
Answer:

V_A=2.5 V	
Transistor	Mode
Qn1	A
Qn2	A
QmR	A
QmO	A

Outline:

At V_A = 2.5 V, the output voltage of the DA is close to $2 \times 2.5 = 5$V. The current in the output transistor is then 5V/1132 = 4.4 mA. and this transistor is active. V_{CB} for Qn1 is 7.5 V and it carries the remainder of the mirror current, so it is active. The DA emitter voltage will follow V_A so it is above the mirror base voltage and the mirror is above its compliance voltage. Therefore, QmO is active. QmR always is active.

Problem 2: Two-port problem



.model Q_n NPN (Is={I_s} Bf={B_f} Vaf={V_af})

FIGURE 2

Two-stage amplifier to be analyzed as a two-port

Figure 2 shows a voltage amplifier. The small-signal behavior of the amplifier of Figure 2 is to be analyzed using two-ports. Load R_L is not part of the amplifier.

1. Construct a small-signal circuit as a cascade of two ports, one for each stage individually; sketch your two-ports with components labeled. In your outline, derive the formulas for the components.

Answer:

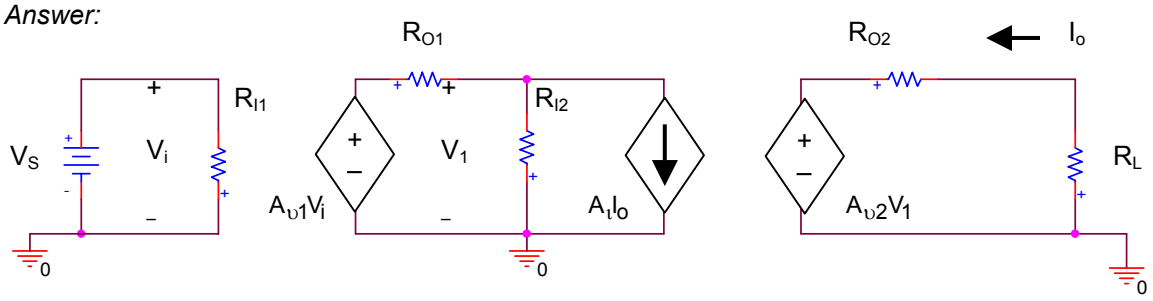


FIGURE 3

Assembly of the two two-ports attached to the load R_L

Component values are found below to be:

$A_{\upsilon 1} = \frac{\beta(R_C \,//\, r_O)}{2r_\pi}$; $R_{I1} = 2\, r_\pi$; $R_{O1} = \frac{1}{2}\{R_C \,//\, r_O + R_C \,//[r_\pi + (\beta+1)r_O]\}$ with r_O and r_π for Stage 1

$A_{\upsilon 2} = \frac{1}{1+\frac{r_\pi}{(\beta+1)r_O}}$; $A_\iota = -\frac{1}{\beta+1}\left(\frac{1}{1+\frac{r_\pi}{(\beta+1)r_O}}\right)$; $R_{I2} = r_\pi + (\beta+1)r_O$; $R_{O2} = \frac{r_\pi}{(\beta+1)} \,//\, r_O$ with r_O and r_π for Stage 2

Outline:

DIFFERENTIAL AMPLIFIER – STAGE1

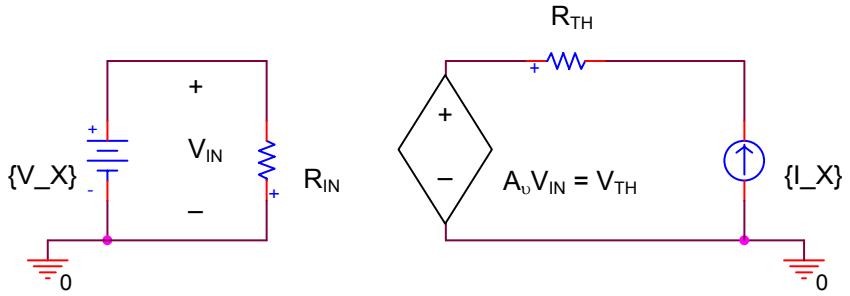


FIGURE 4

Two-port for differential amplifier

Figure 4 shows the two-port for the differential amplifier. If the input voltage is 1V, the open-circuit output voltage is the Thevenin voltage for the circuit; so finding A_υ is the same as finding the Thevenin voltage. Likewise, the output resistance is found by shorting the input voltage and applying a test current at the output; that is, the output resistance is simply the Thevenin resistance of the circuit. Because the driving voltage has no series resistance, the input resistance has no effect on the amplifier.

Finding the output resistance

Strictly speaking the amplifier is not symmetric because of the base current of the VF stage, which makes the collector currents slightly different, causing r_O and r_π to differ on the two sides. According to the currents in Figure 2, this error is about 8/9906 ≈ 0.09%. We neglect this mismatch to make the even-odd superposition approach possible.

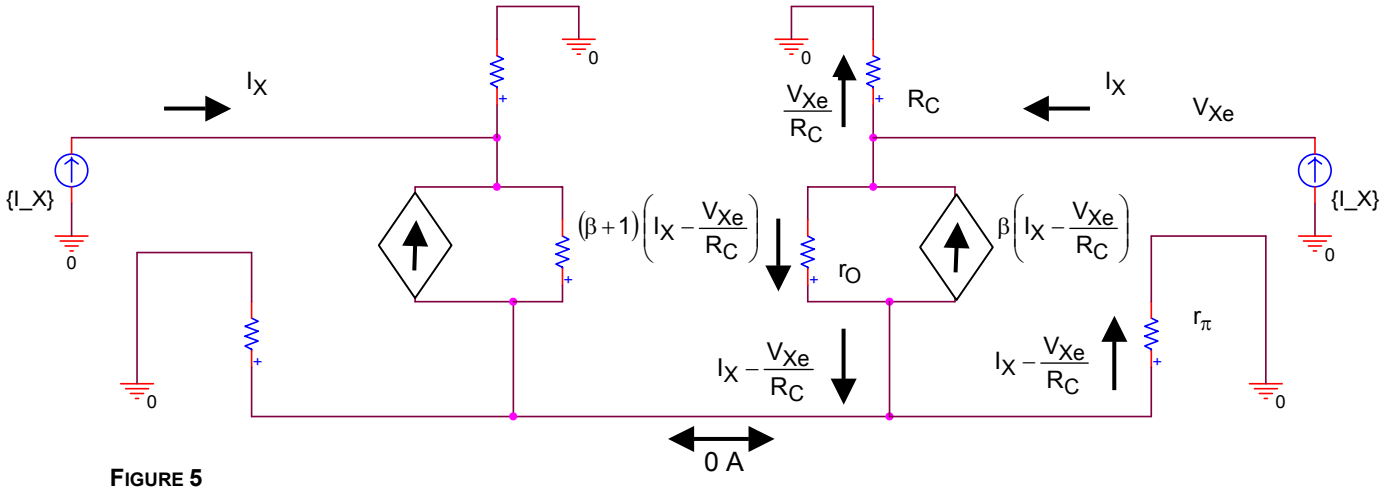


FIGURE 5

Even-mode excitation; by symmetry the current in the center of the emitter is zero

Using the even-mode excitation, we use KCL to establish that the base current is as shown. The base current along with KCL determines all the other branch currents. Then KVL from the test current to ground through r_π determines V_{Xe} as (subscript "e" for even mode)

EQ. 8

$$V_{Xe} = \left((\beta+1)r_O + r_\pi\right)\left(I_X - \frac{V_{Xe}}{R_C}\right);$$

and collecting terms we find

EQ. 9

$$V_{Xe} = I_X R_C \,//\left\{r_\pi + (\beta+1)r_O\right\}.$$

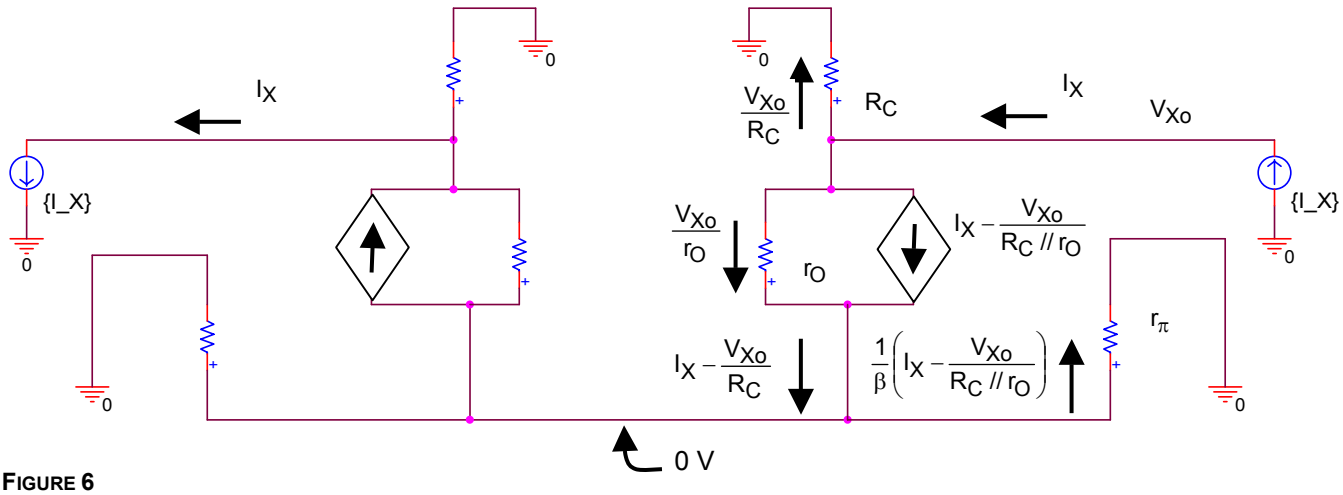


FIGURE 6

Odd-mode excitation; by symmetry the voltage in the center of the emitter is zero

Using the zero emitter voltage, we find the current in the output resistance and then use KCL to find the other branch currents. KVL from the emitter to ground provides EQ. 10 below.

EQ. 10

$$0 = \frac{1}{\beta}\left(I_X - \frac{V_{Xo}}{R_C /\!/ r_O}\right) r_\pi ,$$

or

EQ. 11

$$V_{Xo} = I_X R_C /\!/ r_O .$$

We now superpose the two solutions to obtain the situation shown in Figure 7.

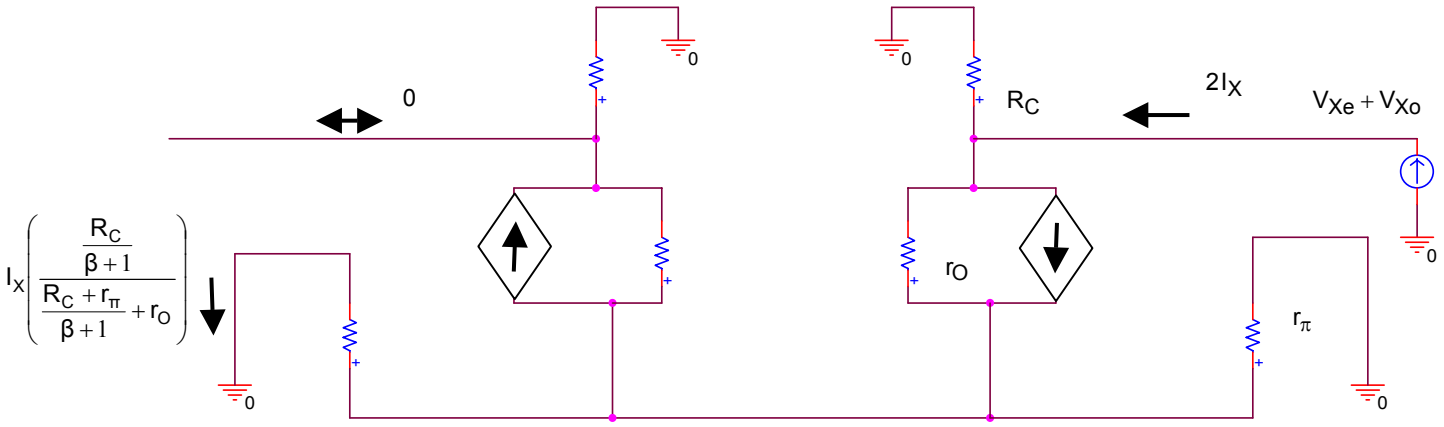


FIGURE 7

Superposing the two solutions with the same values of I_X, I_X on the left side adds to zero, producing the one-sided excitation appropriate for finding the Thevenin resistance

Making the currents I_X the same for even and odd excitations, the two cancel on the input side and add to 2 I_X on the output side. The output resistance is then

EQ. 12

$$R_O = \frac{V_{Xe} + V_{Xo}}{2I_X} = \frac{1}{2}\left\{R_C /\!/ r_O + R_C /\!/ \left[r_\pi + (\beta + 1) r_O\right]\right\}.$$

Incidentally, the current flowing to ground at the left of Figure 7 shows that the circuit of Figure 4 should include a CCCS on the left side to account for feedback due to asymmetry. This feedback is small (r_O >> $R_C/(\beta+1)$), and I have neglected it in Figure 4.

FINDING THE GAIN

Again, we assume no mismatch of the transistors and neglect the imbalance introduced by the VF base current.

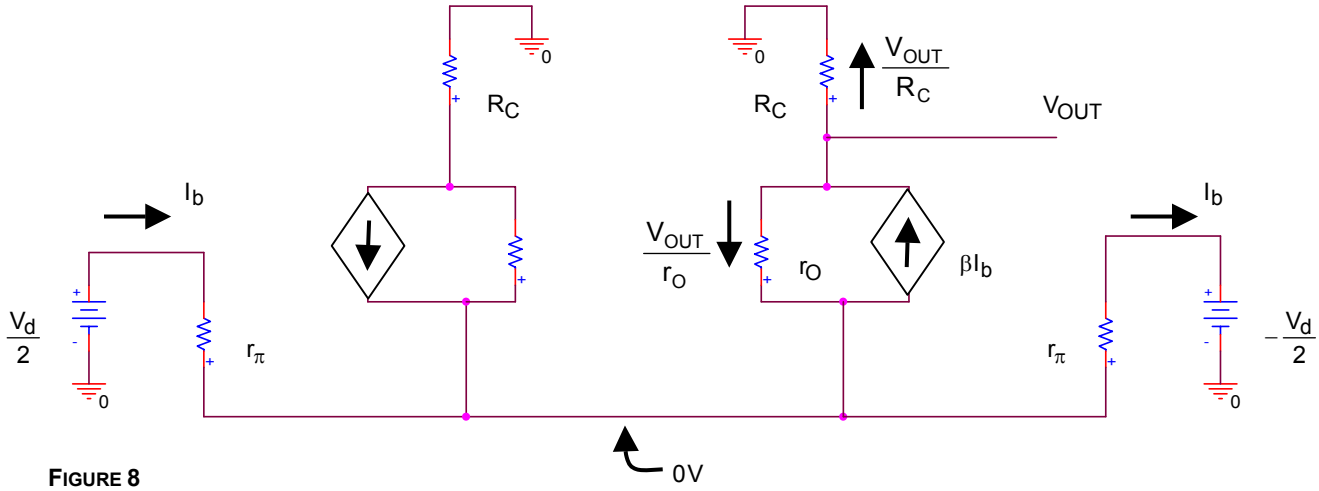


FIGURE 8

Standard difference mode excitation of differential amplifier

Using Figure 8, EQ. 13 below provides the input resistance:

EQ. 13

$$R_{IN} = 2\,r_\pi$$

and we find the output voltage is

EQ. 14

$$V_{OUT} = \frac{\beta(R_C \,//\, r_O)}{2r_\pi} V_d = A_\upsilon V_d$$

We now have all the components of the two-port in Figure 4.

VOLTAGE-FOLLOWER AMPLIFIER – STAGE2

This example was done in class. The two-port is shown in Figure 9.

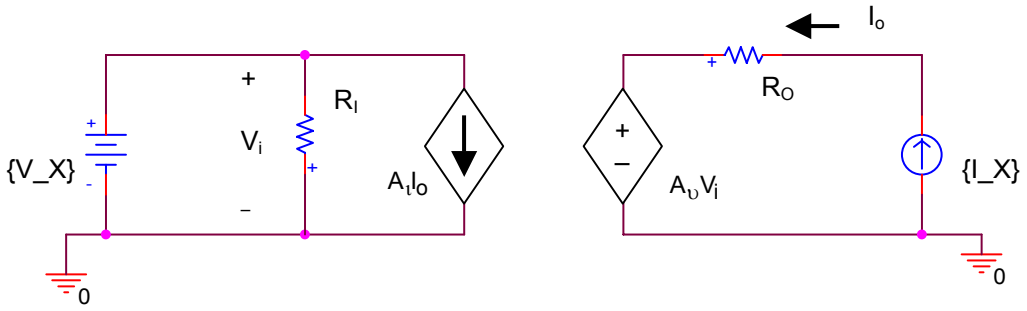


FIGURE 9

Two-port for voltage follower

The input and output resistances are found using the reflection rules, as shown in class, and are

EQ. 15

$$R_I = r_\pi + (\beta+1) r_O\,; \quad R_O = \frac{r_\pi}{(\beta+1)} \,//\, r_O\,.$$

The voltage and current gains are given by the small-signal analysis in class as

EQ. 16

$$A_\upsilon = \frac{1}{1+\dfrac{r_\pi}{(\beta+1)r_O}}\,; \qquad A_\iota = -\frac{1}{\beta+1}\left(\frac{1}{1+\dfrac{r_\pi}{(\beta+1)r_O}}\right).$$

2. Consolidate the two two-ports into one two port; derive and label components

Answer:

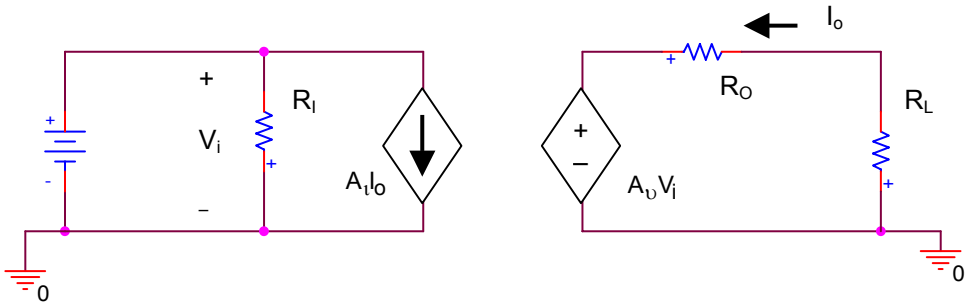


FIGURE 10

A two-port for the complete amplifier attached to the load R_L

The components of Figure 10 in terms of those in Figure 3 are:

$$A_\iota = 0\ \text{A/A};\ R_O = -A_{\upsilon 2}A_{\iota 2}(R_{O1} /\!/ R_{I2}) + R_{O2};\ A_\upsilon = A_{\upsilon 1}A_{\upsilon 2}\frac{R_{I2}}{R_{I2}+R_{O1}};\ R_I = R_{I1}$$

Outline:

We put the two-ports together as shown in Figure 3. Then we make an equivalent two-port for the whole thing, as shown in Figure 10 above. The components of Figure 10 are found using the standard procedure; that is, we look at two different terminations, each designed to eliminate one dependent source. The hardest case to solve is with input shorted and a test current at the output, as seen in Figure 11.

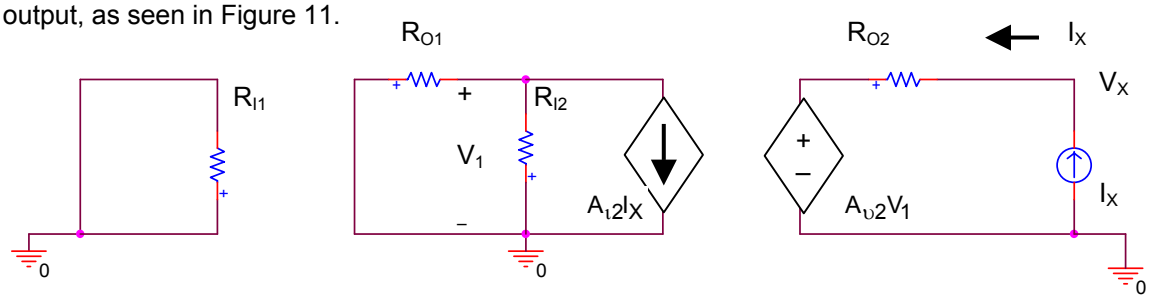


FIGURE 11

Finding A_ι and R_O for circuit of Figure 10

We find zero current in the shorted input lead, so $A_\iota = 0$ A/A in Figure 10. We find $V_1 = -A_{\iota 2}(R_{O1}/\!/R_{I2})\ I_X$. Therefore, $V_X = A_{\upsilon 2}V_1 + I_X R_{O2} = -A_{\upsilon 2}A_{\iota 2}(R_{O1}/\!/R_{I2})\ I_X + I_X R_{O2}$. Therefore,

EQ. 17

$$R_O = \frac{V_X}{I_X} = -A_{\upsilon 2}A_{\iota 2}(R_{O1} /\!/ R_{I2}) + R_{O2}\,.$$

Open-circuiting the output and applying a test voltage at the input determines the other components.

3. Collapse the two-ports into a Thevenin voltage driver for the load R_L; derive and label components.

Answer:

The Thevenin equivalent circuit is shown in Figure 12 below. We find $R_{TH} = R_O$ and $V_{TH} = A_\upsilon V_S$, with R_O and A_υ from Figure 10.

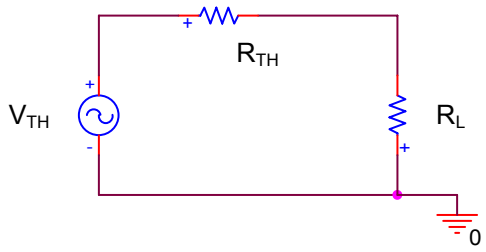


FIGURE 12
Thevenin equivalent for amplifier attached to the load R_L

Outline: We use the standard approach to make a Thevenin circuit equivalent to the circuit of Figure 10. Because A_ι in Figure 10 is zero, $R_{TH} = R_O$ and $V_{TH} = A_\upsilon V_S$.

4. Evaluate the voltage gain using the Thevenin circuit, by formula and numerically.

Answer: The formulas already have been given in earlier parts.

The gain using the Thevenin circuit is

EQ. 18

$$\frac{V_O}{V_S} = \frac{V_O}{V_{TH}} \frac{V_{TH}}{V_S} = \frac{R_L}{R_{TH} + R_L} A_\nu \, .$$

The numerical evaluation is V_O/V_S = 87.76 V/V.

Outline:

We first evaluate the small-signal parameters.

STAGE 1

$\beta = \beta_o(1+V_{CB}/V_{af}) = 100\ (1+5/50) = 110$

$r_\pi = \beta V_{TH}/I_C = 110 \times 25.864\text{mV}/9.91\text{ mA} = 287.1\ \Omega$

$r_O = (V_{CB}+V_{af})/I_C = (5+50)/9.91\text{mA} = 5.55\ \text{k}\Omega$

STAGE 2

$\beta = \beta_o(1+V_{CB}/V_{af}) = 100\ (1+5/50) = 110$

$r_\pi = \beta V_{TH}/I_C = 110 \times 25.864\text{mV}/9.91\text{ mA} = 287.1\ \Omega$

$r_O = (V_{CB}+V_{af})/I_C = (5+50)/9.91\text{mA} = 5.55\ \text{k}\Omega$

These values are the same as for stage 1.

Then we evaluate the two-port parameters, and finally the Thevenin parameters. A spreadsheet listing is below.

		R_L	1.00E+08
		R_C	500
		V_th	0.025864
		B_f	100
		I_C	9.91E-03
		V_af	50
	B_ac*V_th/I_C	r_PI	287.0878
	r_PI/(B_ac+1)	r_E	2.586376
	(V_CB+V_af)/I_C	r_O	5549.95
		V_CB	5
Beta with V_CB	B_f*(1+V_CB/V_af)	B_ac	110
	1/(1/R_C+1/r_O)	RC_rO	458.6773
Stage 1	B_ac*RC_rO/(2*r_PI)	A_v1	87.87296
	2*r_PI	R_I1	574.1756
	0.5*(RC_rO+1/(1/R_C+1/(r_PI+(B_ac+1)*r_O)))	R_O1	479.136
Stage 2	1/(1+r_PI/((B_ac+1)*r_O))	A_v2	0.999534
	r_PI+(B_ac+1)*r_O	R_I2	616331.5
	1/(1/r_E+1/r_O)	R_O2	2.585172
	-(1/(B_ac+1))*(1/(1+r_E/r_O))	A_I2	-0.009
Output R of combined two-port	-A_v2*A_I2*(1/(1/R_O1+1/R_I2))+R_O2	R_Oc	6.894342
	R_I1	R_I	574.1756
	A_v1*A_v2*R_I2/(R_I2+R_O1)	A_v	87.7638
Gain using Thevenin	A_v*R_L/(R_L+R_Oc)	Gain	87.76379

FIGURE 13
Spreadsheet listing of all parameters