ECE 304 Spring '06 First Exam Solutions

For all problems take the thermal voltage as V_{TH} = 25.864 mV.

Problem 1: Current mirror

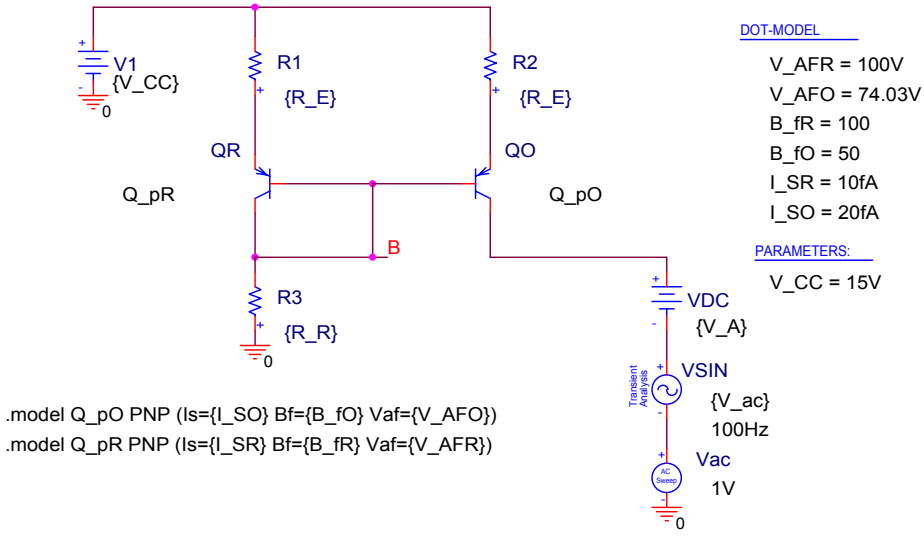


FIGURE 1

Current mirror for Problem 1

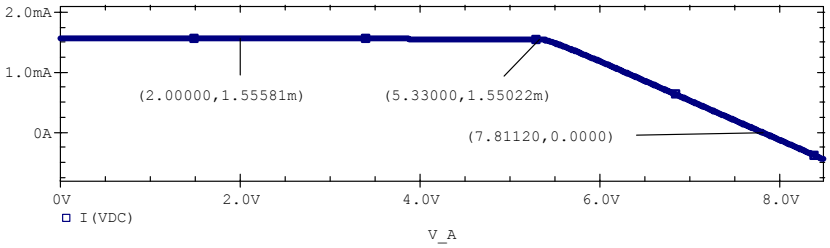


FIGURE 2

Current vs. DC voltage for current mirror of Figure 1

1. Select values for R_R and R_E so the mirror will have the *I-V* behavior seen in Figure 2. Assume the maximum forward CB bias in saturation is $V_{CB} = V_{SAT}$ = 500 mV

Answer: R_E = 6 kΩ , R_R = 3 kΩ

Outline:

Find R_E: From the *I-V* plot, the compliance voltage is V_{CV} = 5.33 V. At $V_A = V_{CV}$, the collector is above the base by V_{SAT} = 0.5 V. Therefore, the base voltage is V_B = 5.33 – 0.5 = 4.83 V. The current at V_{cv} is 1.55 mA. Figure 2 shows that this current will not change significantly at $V_A = V_B$, so we can find the emitter-base voltage as $V_{EB} = V_{TH}\ell n\,(I_C/I_S)$ = 25.864 mV ℓn(1.55m/20f) = 0.6485 V. The leg resistor value from KVL down the output leg of the mirror is then $R_E = (V_{CC}–V_{EB} – V_B)/(1+1/\beta)I_C$ = 6 kΩ.

Find R_R: Let the collector current on the reference side be I_R. Then V_{EB} on the reference side is $V_{EB}= V_{TH}\,\ell n\,(I_R/I_{SR})$. As a first guess take $V_{EB} \approx V_{EB}$ on the output side, or V_{EB} ≈ 648.5 mV. Then $I_R = (V_{CC}–V_{EB}-V_B)/(R_E(1+1/\beta_R))$ = (15-.648-4.83)/(6k(1+1/100)) = 1.571 mA → V_{EB} = 666.7 mV → I_R = 1.568 mA. The current through R_R is then $I_R(1+1/\beta_{fR}) + I/\beta_{fO}$ = 1.568mA(1.01) + 1.55m/50 = 1.615 mA and $R_R = V_B/I$ = 4.83/1.615mA = 2.99 kΩ ≈ 3 kΩ.

2. Why does the slope of the *I-V* curve change at large values of V_A?

Answer: The slope changes at large V_A because the output transistor is driven into saturation. That causes the base voltage of the mirror to obey $V_B = V_A–V_{sat}$, so the current through the leg resistor on the output side becomes $(V_{CC}–V_{EB}–V_A + V_{sat})/R_E$, which drops linearly with V_A, making the output current of the mirror drop as well. In addition, the voltage drop across R_R increases

linearly with V_A, drawing increased base current from the output transistor, further reducing the mirror current.

Problem 2: CE amp with current mirror load

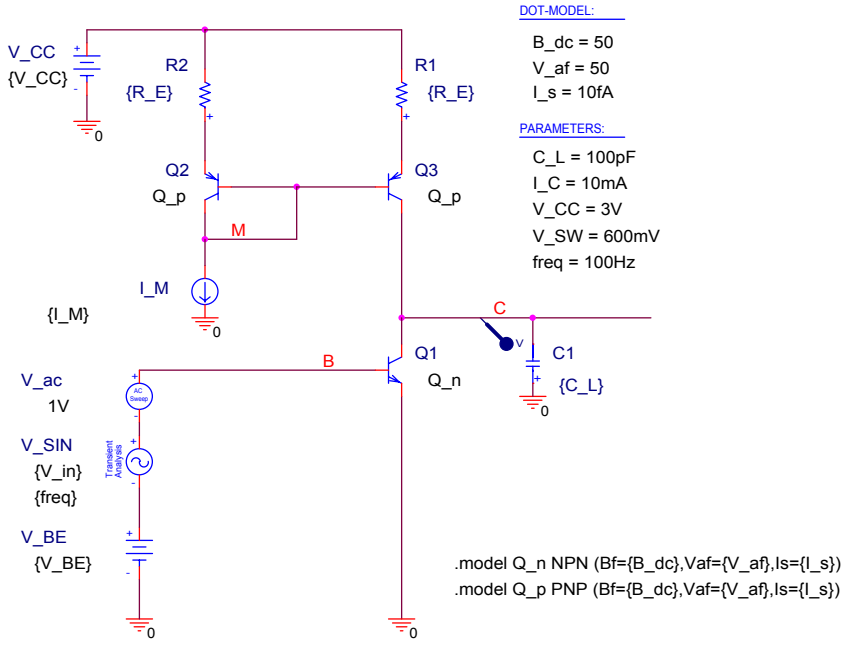


FIGURE 3
CE amplifier with current mirror load

The amplifier of Figure 3 is to be designed to meet these specifications:

- Symmetric output voltage swing of up to 600 mV; to avoid distortion, forward bias of collector-base junctions is to be avoided entirely
- Output (collector current) at Q-point of I_C = 10 mA
- Maximum AC gain compatible with the above two specifications

Do the following:

1. Find V_{BE} at the base (formula and numerical value)

Answer: $V_{BE} = V_{TH}\ell n(I_C@V_{CB}=0/I_S) = 714.6$ mV

Outline: The collector current is 10 mA. The collector current hardly charges when V_{CB} changes 600 mV because of the large mirror resistance. Therefore, at zero V_{CB} we find $V_{BE} = V_{EB} = V_{TH}\ \ell n$ (10mA/10f) = 714.6 mV.

2. Find the DC output voltage V_C (formula and numerical value)

Answer: $V_C = V_S + V_B = 1.315$ V.

Outline: The base voltage of the NPN transistor is V_{BE} = 714.6 mV. The swing is 600 mV. Therefore, the output voltage must be 600 mV above the base, and V_C = 714.6m + 600 m = 1.315 V

3. Find required leg resistors in the mirror R_E (formula and numerical value)

Answer: $R_E = (V_{CC}–V_{EB}–V_B)/I_{OE} = 36.13\ \Omega$

Outline: To obtain maximum gain, the load resistance R_N must be as large as possible. Increasing R_E as far as the swing limit allows increases this resistance. The swing limit of 600 mV places the base of PNP at V_{Bp} =600 mV above the collector or at 1.915 V. The voltage drop across the leg resistor is then $V_{CC} – V_{EB} – V_{Bp}$ = 3 – 0.7146–1.915 = 0.3704 V. The current in the leg resistor on the output side is $I_C(1+1/\beta)$ and $\beta = \beta_{dc}(1+0.6/50) = 50.6 \rightarrow$ current = 10 mA (1+1/50.6) = 10.20 mA. Therefore, R_E = 0.3704 V/ 10.20 mA = 36.31 Ω.

4. Find required mirror bias current I_M (formula and numerical value)

Answer :$I_M = I_R(1+1/\beta_R)+I_O/\beta_O = 11.14$ mA.

Outline: Find the current on the reference side as $I_R = (V_{CC}–V_{EB} – V_B)/((1+1/\beta_{dc})R_E)$. Guess V_{EB} is the value on the output side, 714.6 mV. Then I_R = (3–.7146–1.915)/(33.67× 1.02) = 10.785 mA →

$V_{EB} = V_{TH}\,\ell n(10.785m/10f) = 716.6$ mV $\rightarrow I_R = (3–.7166–1.915)/(33.67 \times 1.02) = 10.727$ mA. The mirror current is then $I_M = I_R(1+1/\beta_{dc}) + I_O/\beta_O = 10.727$ mA(1.02) + 10m/50.6 = 11.14 mA.

5. Find the small-signal voltage gain (formula and numerical value).

Answer: $A_\upsilon = -g_m r_{On}//R_N = -1.78$ kV/V

Outline: Following the steps used in class, the gain is given by $A_\upsilon = -g_m\, r_{ON}//R_N$. The mirror Norton resistance is found as done in class to be

$R_N = r_{Op}(1+\beta R_E/D)+R_E(r_\pi+r_E+R_E)/D$ where $D \equiv r_\pi+r_E+2R_E$.

We find the various resistor values as follows:

$r_E = V_{TH}/(I_R(1+1/\beta_{dc})) = 25.864$mV/(10.727m $\times$ 1.06) = 2.27 Ω

$r_\pi = \beta V_{TH}/I_C = \beta_{dc}(1+V_{CB}/V_{af})\, V_{TH}/I_C = 50(1.012)\times$ 25.864m /10m = 130.9 Ω

$r_{Op} = (V_{CB}+V_{af})/I_C = (0.6 + 50)/10$m = 5.06 k$\Omega$

$R_E = 36.13\ \Omega$

$g_m = I_C/V_{TH} = 10$mA/25.864m = 0.3866 A/V

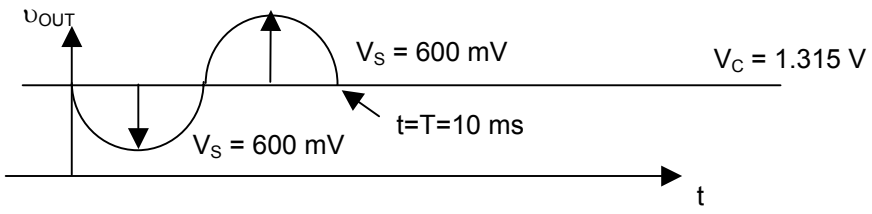
Therefore, D = (130.9 + 2.27 +2 $\times$ 36.1) = 205.4 Ω and $R_N = 5.06$k (1+50.6 $\times$ 36.1/D) + 36.1(130.9 + 2.27 +36.1)/D) = 50.1 kΩ. $r_{ON}//R_N = 5.06$k//50.1k = 4.60k. $A_\upsilon = -0.3866 \times 4.6$k = 1.78 kV/V.

6. Sketch the output voltage vs. time for the case of a sinusoidal input voltage with the maximum amplitude V_in that leaves the transistor Q1 in active mode throughout the cycle. That is, the input voltage is

$$\upsilon(t) = V\_in\, \sin(2\pi t/T)$$

where T = period of signal, taken as 10 ms. Label maximum and minimum voltages.

Answer:



Outline:

The signal swings approximately 600 mV up and down about the DC output voltage, with phase opposite to the input signal.

7. Determine the numerical value for the maximum input amplitude V_{in} that avoids clipping, assuming the above input signal, and the corresponding maximum output upswing and downswing voltage

Answer: $V_{in} = V_S/A_\upsilon = 337\ \mu$V

Outline: The input swing is the output swing divided by the gain, assuming a linear operation. Therefore, $V_{in} = 600$mV/1.78 kV = 337 μV

8. Find the 3 dB bandwidth of the amplifier

Answer: $f_{3dB} = 1/(2\pi C_L r_{On}//R_N) = 346$ kHz

Outline: The output capacitor and the resistance it sees determine the time constant. Following the approach in class, this resistance is shown to be $r_{ON}//R_N$. Therefore the 3dB bandwidth is $f_{3dB} = 1/(2\pi C_L(r_{ON}//R_N)) = 1/(2\pi\ 100$ pF $\times$ 4.6 kΩ) = 346 kHz.

9. Should we expect any distortion if the transistors stay active? Explain.

Answer: Yes, we should because the amplifier is nonlinear, and its gain varies with the output voltage. Thus, as the output swings up and down the gain varies, causing different amplification at different times of the cycle.

10. Discuss the practicality of this circuit

Answer: The circuit is not practical because positioning of the output voltage to obtain good up and downswing depends critically upon a precise value for the base bias V_{BE}. The V_{BE}-value needed depends on temperature and on transistor properties, such as I_S, V_{af} or β_f. Because of the large gain, even small changes in these parameters require a slightly different V_{BE}, or they will cause the output voltage to shift a lot, causing clipping of the output signal. Holding V_{BE} within these tolerances is impractical, and design requires a custom value for each individual circuit.