ECE 304 Final Exam Spring `04
11 AM – 1PM Closed Book

NOTE: In all cases
1. Put your answer first, and
2. Follow up with an outline of your solution. Each major step in the outline should
   2.1. Begin with a heading that describes the objective of that step, and should
   2.2. Have a body where actual work is done, not just hand waving, and should
   2.3. Conclude with a quantitative statement of the major result for that step (a number or formula or both).

For all problems take the thermal voltage as V_{TH} = 25.864 mV.

Problem 1

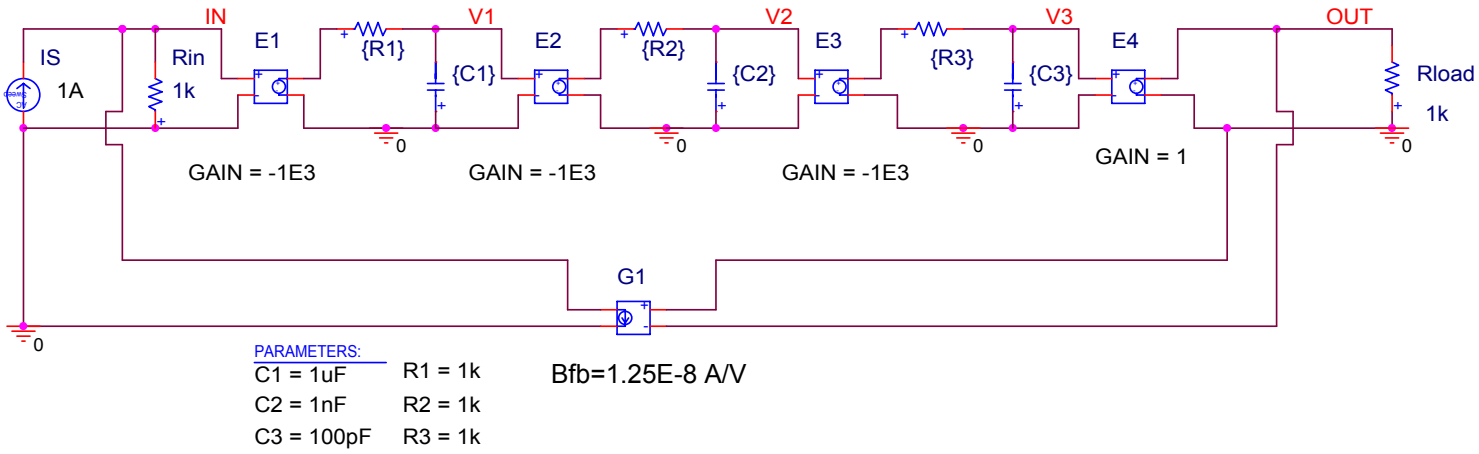

FIGURE 1
Three-pole amplifier in a feedback circuit

For the circuit of Figure 1 select a new value of C_1 so the amplifier operates with a phase margin of 45° when the feedback $\beta_{FB} = 1.25 \times 10^{-8}$ A/V. All resistors are 1 kΩ, and the gains of VCVS E1, E2, E3 are -10^3 V/V. The last VCVS E4 has unity gain. The feedback VCCS has a gain $\beta_{FB} = 1.25 \times 10^{-8}$ A/V. Capacitor C_2 = 1 nF, C_3 = 100 pF.

For the given values of R and C the pole frequencies are f_1 = 159.15Hz, f_2 = 159.15 kHz, and f_3 = 1.5915 MHz.

Follow the outline procedure at the top of the exam with headings for each major step in the solution. No points for answer without an outline of the solution. A mish-mash of calculations is not an acceptable outline.

Problem 2

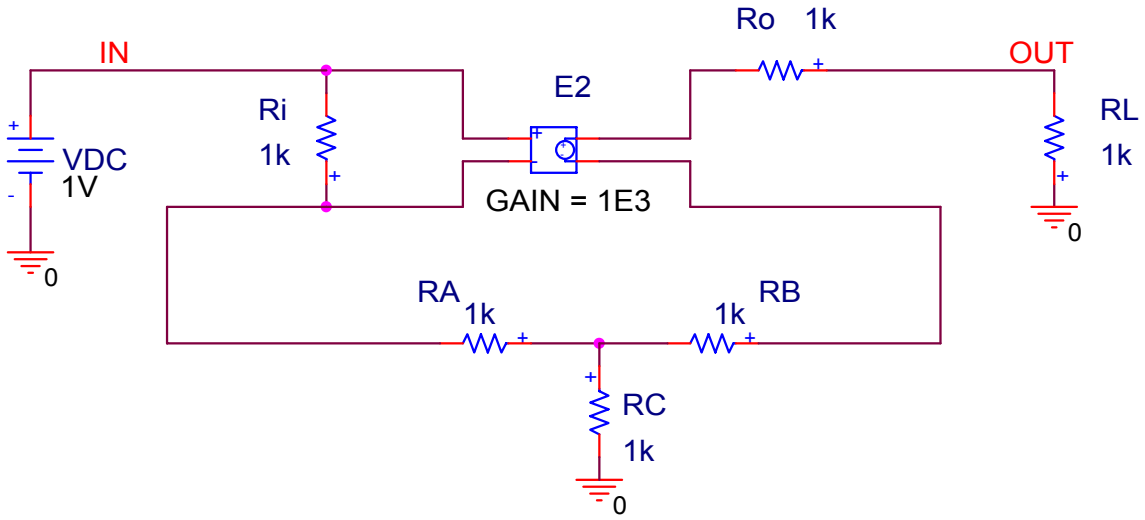

FIGURE 2
Feedback amplifier; gain of main stage from part E2 is 1000V/V

In Figure 2 all resistors are 1 kΩ and the main amplifier has a gain of 1kV/V.

1. Determine the gain of the amplifier with feedback and its units.
2. State which resistors could be eliminated from the feedback T-section and say why.

Follow the outline procedure at the top of the exam with headings for each major step in the solution. No points for answer without an outline of the solution. A mish-mash of calculations is not an acceptable outline.

Problem 3

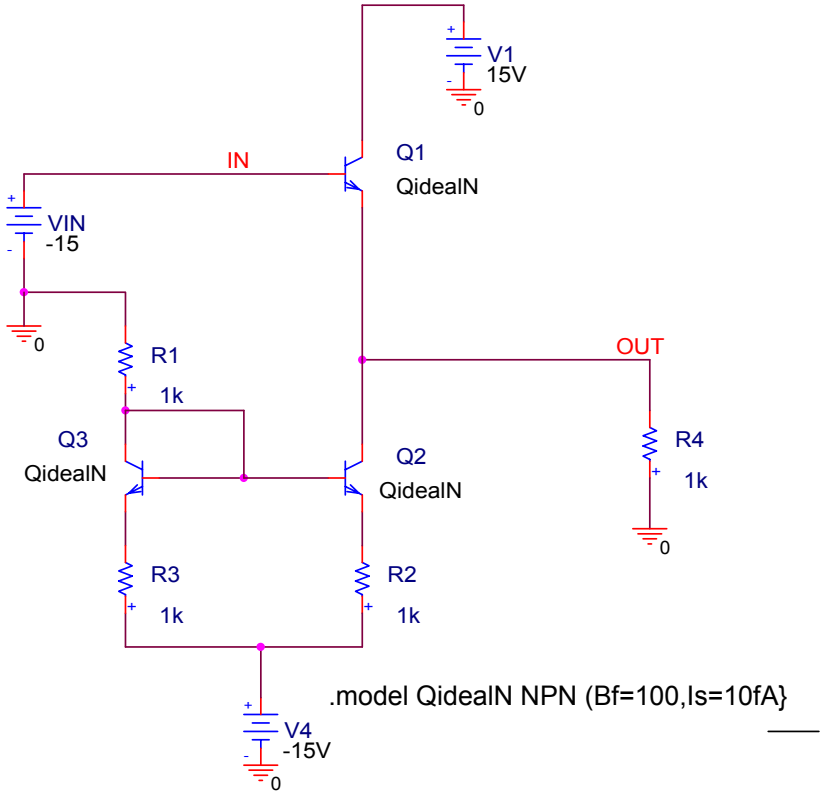

FIGURE 3
Voltage follower stage

For the circuit of Figure 3, determine the DC value of V_{OUT} for a DC input voltage of V_{IN} = –15V.

Follow the outline procedure at the top of the exam with headings for each major step in the solution. No points for answer without an outline of the solution. A mish-mash of calculations is not an acceptable outline.

Problem 4

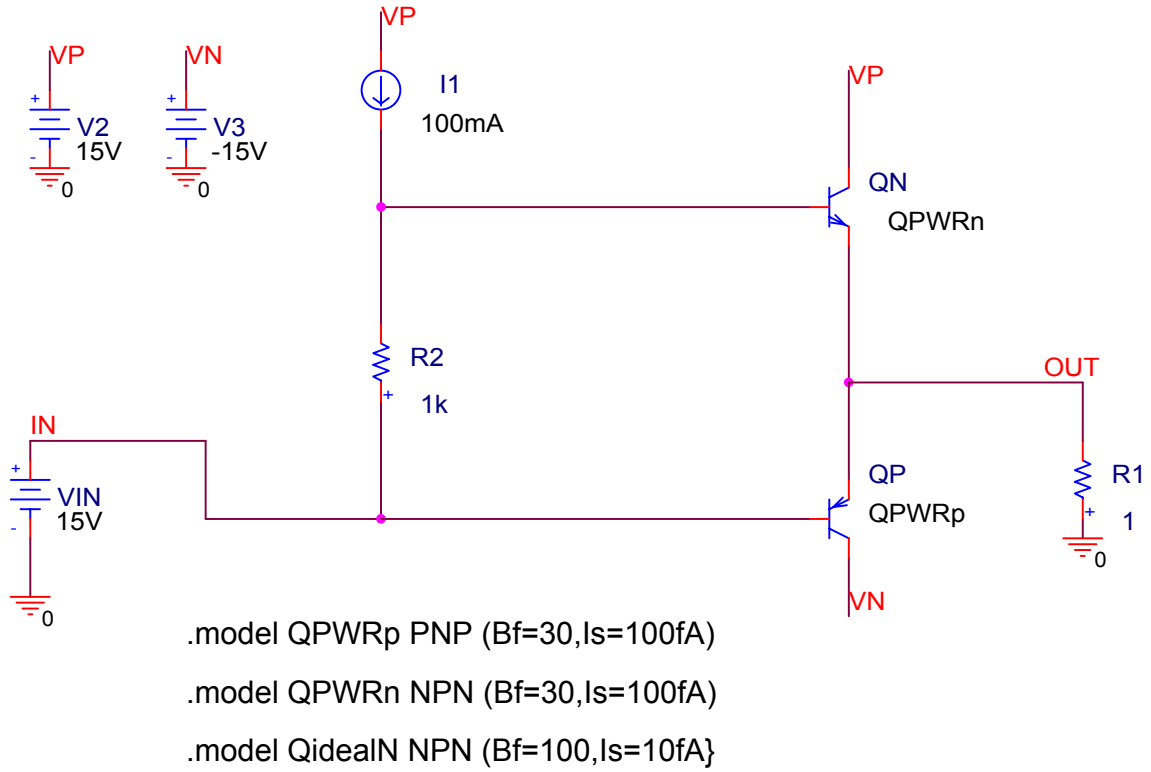

FIGURE 4
Power output amplifier

For the circuit of Figure 4, determine the DC value of V_{OUT} when the DC value of V_{IN} = 15 V.

Follow the outline procedure at the top of the exam with headings for each major step in the solution. No points for answer without an outline of the solution. A mish-mash of calculations is not an acceptable outline.

Problem 5

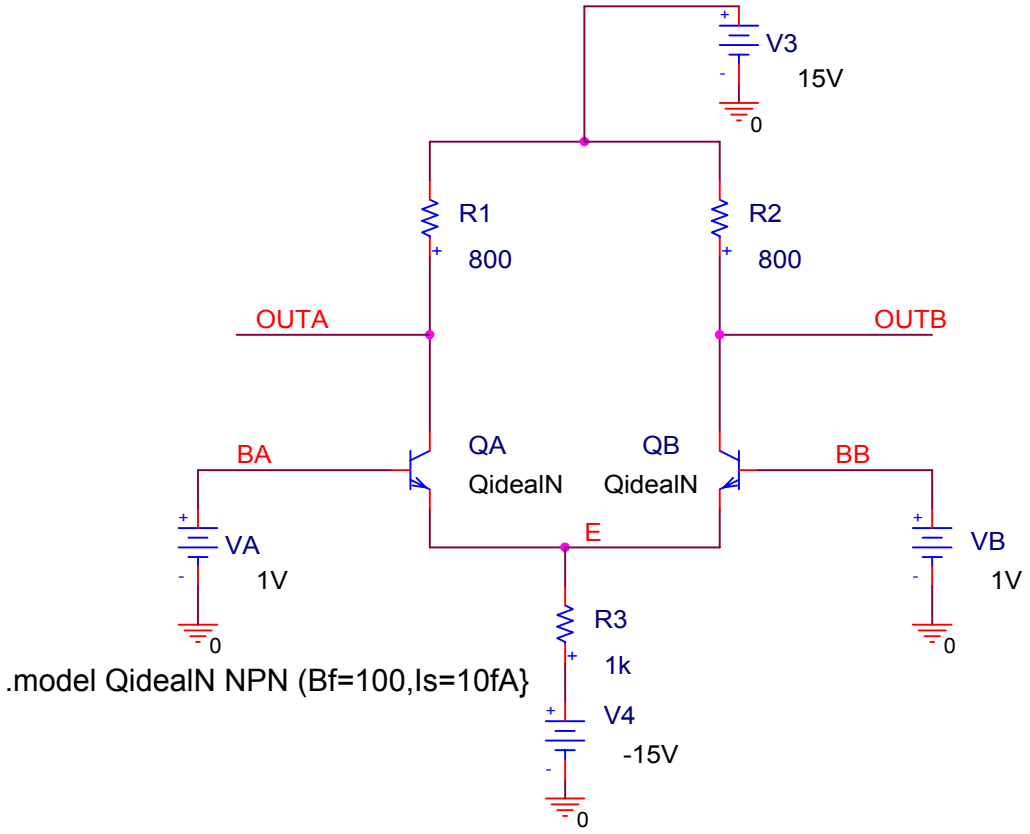

FIGURE 5
Differential amplifier

For the amplifier of Figure 5 assume the maximum forward bias of the CB junction in saturation is $V_{CB} = -V_{SAT} = -600$ mV. Also, assume in active mode $V_{BE} = 700$mV. Make a table like the one below and fill it in.

Do **NOT** use the table on this page.

		Mode	Mode			
VA	VB	QA	QB	VOUTA	VOUTB	VE
7	1					
2	1					
1	1					
0	1					

Provide an outline only for the case $V_A = 2$V. For this case, follow the outline procedure at the top of the exam with headings for each major step in the solution. A mish-mash of calculations is not an acceptable outline.

Problem 6

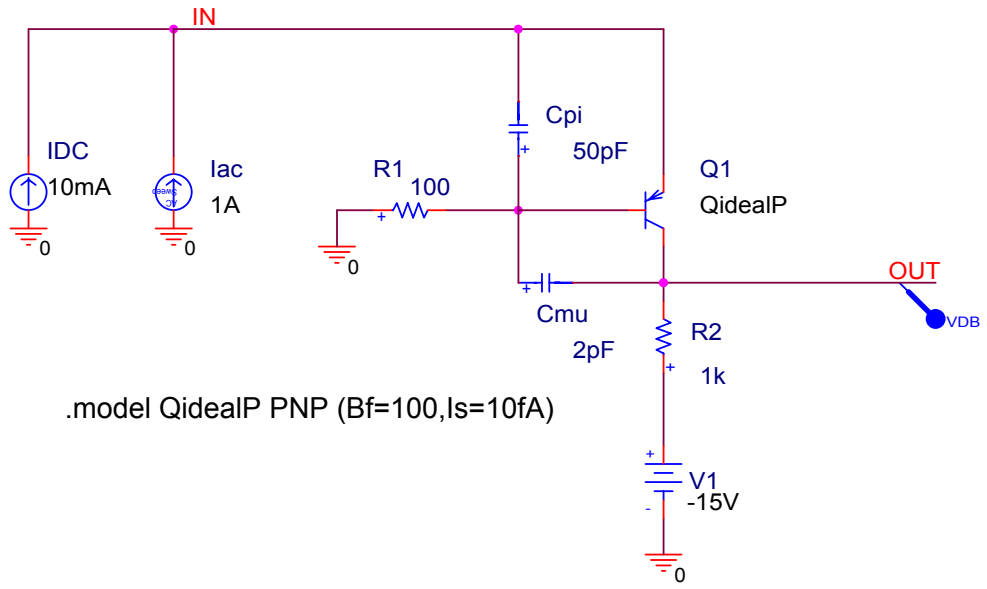

FIGURE 6
Transresistance amplifier

In Figure 6 the transistor parasitic capacitances Cpi ≡ C_π and Cmu ≡ C_μ are shown explicitly as if they were external capacitances with values C_π = 50 pF and C_μ = 2 pF. Determine the upper 3dB corner frequency of the small-signal transresistance gain V_{out}/I_{ac}.

Follow the outline procedure at the top of the exam with headings for each major step in the solution. No points for answers without an outline of the solution. A mish-mash of calculations is not an acceptable outline.