ECE 304: Final Exam Spring `03

Problem 1: Short questions for sketch and word answers (25 pts; ~25 min)

1. Define the classifications of power output amplifiers and describe their trade-offs.
2. Sketch a bipolar cascode circuit.
3. Sketch a pnp-differential amplifier with an npn-active load. Label the output node.
4. What are the advantages of an active load in a differential amplifier?
5. Sketch the current flow pattern in the V_{BE}-multiplier when the output voltage is at its lowest.
6. Describe the open-circuit time constant method and its relation to the midband circuit.
7. List the advantages of negative feedback.
8. List the disadvantages of negative feedback.
9. Sketch the DC common-mode transfer curve for a one-sided differential amplifier biased by a current mirror and identify the modes of the transistors in the mirror and in the differential amplifier in each region of the curve. Label the common-mode range.
10. Sketch the DC difference-mode transfer curve for a one-sided differential amplifier biased by a current mirror and identify the modes of the transistors in each region.

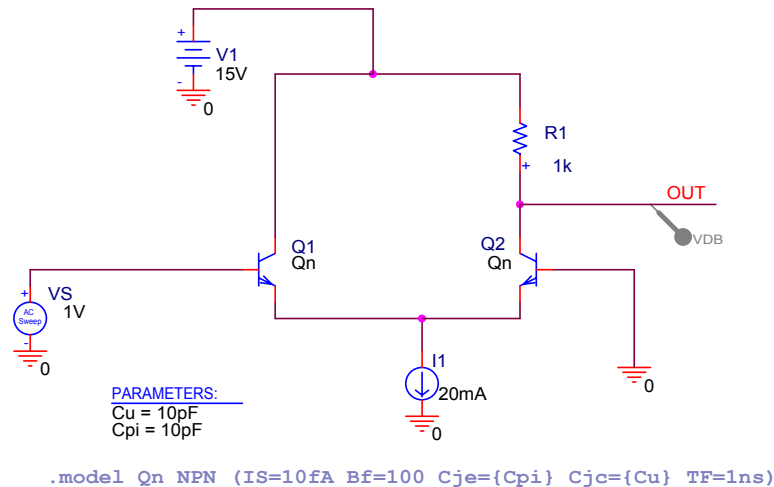**Problem 2: Differential amplifier frequency response (10 pts; ~ 10 min)**

PARAMETERS:
Cu = 10pF
Cpi = 10pF

`.model Qn NPN (IS=10fA Bf=100 Cje={Cpi} Cjc={Cu} TF=1ns)`

FIGURE 1

One-sided differential amplifier

NAME	Q_Q1	Q_Q2
MODEL	Qn	Qn
IB	9.90E-05	9.90E-05
IC	9.90E-03	9.90E-03
VBE	7.14E-01	7.14E-01
VBC	-1.50E+01	-5.10E+00
VCE	1.57E+01	5.81E+00
BETADC	1.00E+02	1.00E+02
GM	3.83E-01	3.83E-01
RPI	2.61E+02	2.61E+02
RX	0.00E+00	0.00E+00
RO	1.00E+12	1.00E+12
CBE	3.99E-10	3.99E-10
CBC	3.66E-12	5.08E-12
BETAAC	1.00E+02	1.00E+02

FIGURE 2

Q-point data for Figure 1; note that r_O can be taken as ∞

For the amplifier in Figure 1 do the following,

1. Assuming $r_O \approx \infty$, determine a formula for the complete frequency dependence (all poles and zeros) of the small-signal voltage gain V_{OUT}/V_S of the differential amplifier of Figure 1

Using the numerical values of Figure 1 and Figure 2

2. Sketch the dB gain plot
3. Sketch the Bode phase plot

Note: Label <u>numerical</u> values of all slopes and label the <u>numerical</u> coordinates of all break points.
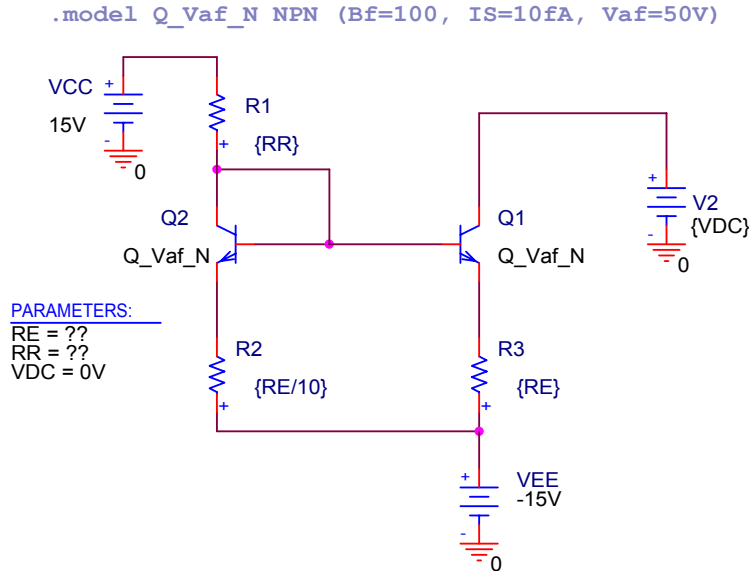
Problem 3: Current mirror design (20 pts; ~ 10 min)

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.model Q_Vaf_N NPN (Bf=100, IS=10fA, Vaf=50V)
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FIGURE 3
  Current mirror; note that the emitter leg resistor on the left is 1/10 that on the right

Select R_E and R_R for the current mirror in Figure 3 to achieve a compliance voltage (relative to ground) of V_{DC} = zero volts at a DC current level of 10 μA. Take V_{TH} = 25.85 mV and use the dot-model parameters to find V_{BE} for each transistor. Assume $I_C \approx I_E$ and <u>zero tolerance</u> of forward bias in saturation. **Note:** The emitter leg resistors have different values.
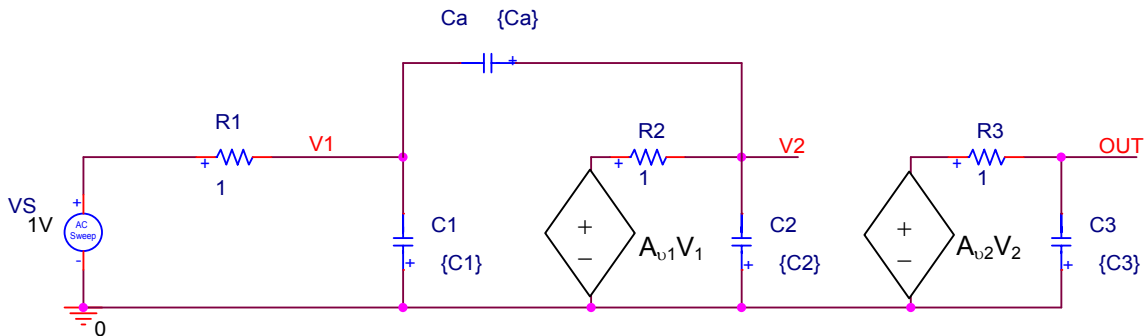
Problem 4 (25 pts; ~ 25 min)

FIGURE 4
 Two-stage amplifier

$$C_1 = 1.592E\text{-}03\ F \qquad A_{v1} = -1.00E\text{+}05\ V/V \qquad R_1 = 1\ \Omega$$
$$C_2 = 1.592E\text{-}05\ F \qquad A_{v2} = -1.00E\text{+}05\ V/V \qquad R_2 = 1\ \Omega$$
$$C_3 = 1.592E\text{-}08\ F \qquad\qquad\qquad\qquad\qquad\quad R_3 = 1\ \Omega$$

FIGURE 5
        Parameter values for two-stage amplifier

For the amplifier of Figure 4 with the parameters of Figure 5, for large values of C_a, the first pole shifts down and the second pole shifts up and locks at 10 MHz. Do the following

1. For a negative feedback amplifier with $1/\beta_{FB} = 10$ dB, determine the position of the lowest pole corresponding to a phase margin of 45° assuming C_a large enough to lock the second pole at 10 MHz.
2. Determine the corresponding value of C_a.
3. Sketch the Bode gain and phase plots for the open-loop amplifier with the new pole positions; label numerical values of all slopes and provide numerical values for the coordinates of all break points
4. On your gain plot show the curve for $1/\beta_{FB}$ and label the numerical value of the coordinates of its intersection with the open-loop amplifier gain curve.
5. On your phase plot label the numerical location of the frequency for 45° phase margin.

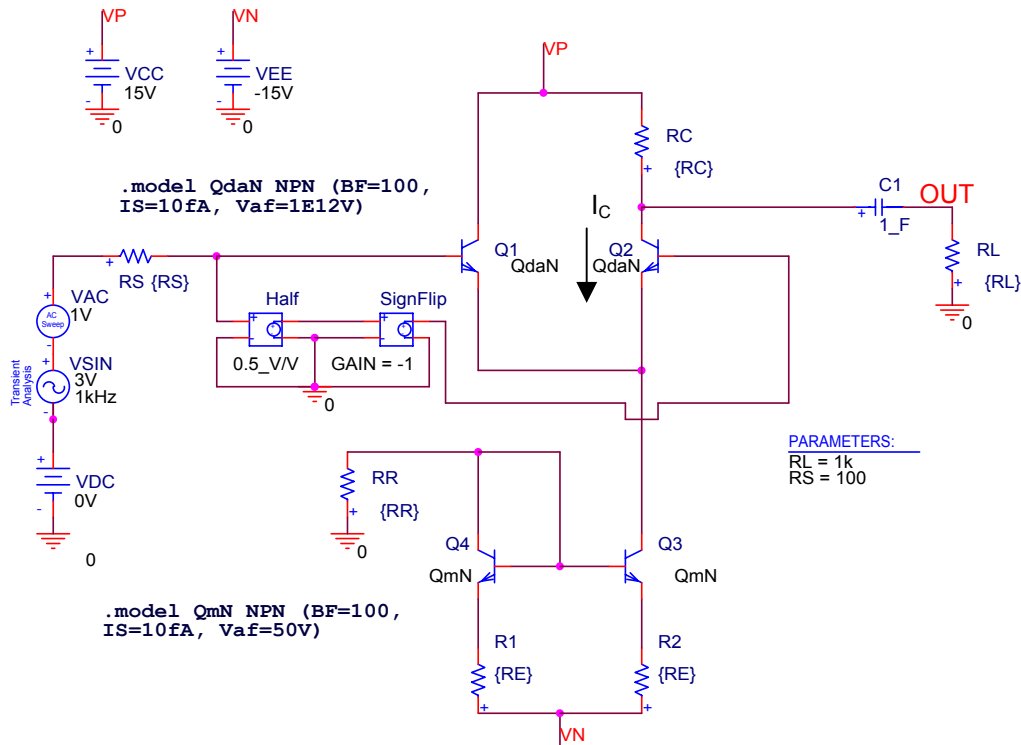**Problem 5: Differential amplifier design (20 pts; ~ 20 min)**

FIGURE 6
        Differential amplifier hooked up in difference mode; $\beta = B_F = 100$; I_C = Q-point bias current

By selecting values of R_R, R_E and R_C, arrange to meet the following specifications:
1. Amplifier allows common-mode input amplitudes from $-6V \leq V_S \leq 6V$
2. Amplifier small-signal difference mode gain V_{OUT}/V_d should be as large as possible
3. Q-point DC current level I_C should provide the best small-signal difference mode gain V_{OUT}/V_d possible
4. Amplifier small-signal common mode gain V_{OUT}/V_c should be as small as possible

The specifications are listed in priority; that is, in any trade-off, the higher priority is listed first. The DA transistors have infinite output resistance to simplify calculations. Assume <u>zero tolerance</u> for forward bias in saturation. Assume $I_C \approx I_E$, V_{BE} = 0.7V and V_{TH} = 25.85mV. Arrange your work as follows:

1. Describe your reasoning for implementing these requirements <u>in this order</u>:
    1.1. How is the upper end of the common-mode range insured?
    1.2. How is the lower end of the common mode range insured?
    1.3. How is the highest DM gain insured?
    1.4. How is the lowest CM gain insured?
    1.5. How is the best value of Q-point collector current I_C of Q2 determined?
2. Show how to calculate the best value of Q-point collector current I_C of Q2.
3. Find the numerical value of the best DC bias current I_C.
4. <u>Tabulate</u> formulas and numerical values for your three resistors as shown in Figure 7.

	RR	RE	RC
Formula			
Numerical value			

FIGURE 7
   Tabulation of resistor determination