ECE 304: Fall '02 Final Exam Solutions

Problem 1

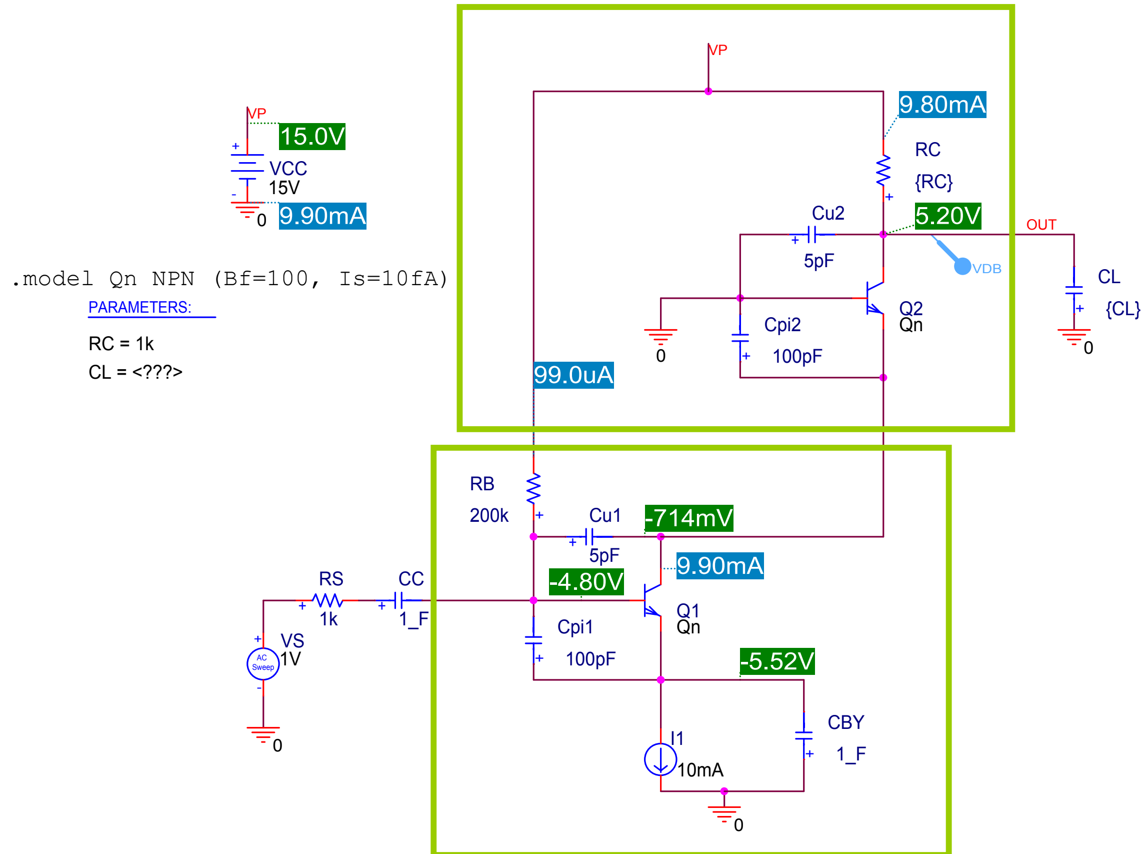

FIGURE 1

Circuit for problem 1; R_S = 1 kΩ, R_C = 1 kΩ, $C_{u1} = C_{u2}$ = 5 pF, and $C_{pi1} = C_{pi2}$ = 100pF

NAME	Q_Q2	Q_Q1
MODEL	Qn	Qn
IB	9.80E-05	9.90E-05
IC	9.80E-03	9.90E-03
VBE	7.14E-01	7.14E-01
VBC	-5.20E+00	-4.09E+00
VCE	5.91E+00	4.80E+00
BETADC	1.00E+02	1.00E+02
GM	3.79E-01	3.83E-01
RPI	2.64E+02	2.61E+02
RX	0.00E+00	0.00E+00
RO	1.00E+12	1.00E+12
CBE	0.00E+00	0.00E+00
CBC	0.00E+00	0.00E+00
CJS	0.00E+00	0.00E+00
BETAAC	1.00E+02	1.00E+02
CBX/CBX2	0.00E+00	0.00E+00
FT/FT2	6.03E+18	6.09E+18

FIGURE 2

Q-point data for Figure 1; C_{BE} and C_{BC} are zero, $r_O = 10^{12}\ \Omega$

The load capacitance C_L represents the <u>high-frequency</u> input capacitance of the following stage.[1] Note that the •model statement of Q1 and Q2 includes <u>no</u> capacitances, so C_μ and C_π are given instead by the external capacitors $C_{u1} = C_{u2} = C_\mu = 5$ pF and $C_{pi1} = C_{pi2} = C_\pi = 100$ pF.

Using the circuit of Figure 1 and the Q-point data of Figure 2, answer the following questions. Marks are apportioned according to difficulty, with part 6 counting the most.

1. What is this circuit named? *Cascode*
2. What is the usefulness of this circuit? *High gain and wide bandwidth with good impedance match for Thevenin driver*
3. How is the usefulness of this circuit achieved? *The CB output stage provides high gain and also high bandwidth because C_μ is grounded on base side leading to a short time constant for the CB stage. The CE input stage serves to convert the driver to a high impedance Norton current source that matches well to the CB stage. The CB stage presents such a low impedance to the CE stage that the CE stage has a gain of about 2V/V, so the Miller effect in the CE stage is unimportant in limiting the bandwidth of the circuit.*
4. Find the Norton equivalent of the combined voltage driver and first stage at midband.

We make a small-signal equivalent of the first stage, and map that into a small-signal Norton equivalent. Ignore R_B, which is too large to make much difference.

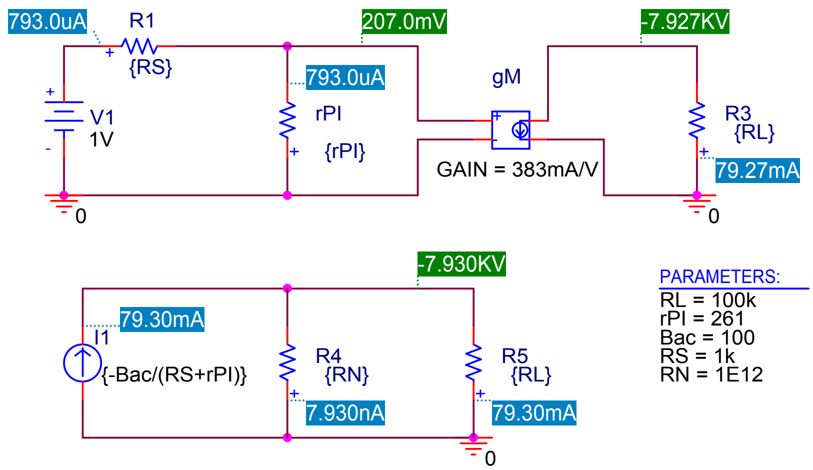

FIGURE 3

Norton equivalent

5. Find the input impedance of the second stage at midband.

We construct the small-signal equivalent of the output stage and put a test voltage at the input.

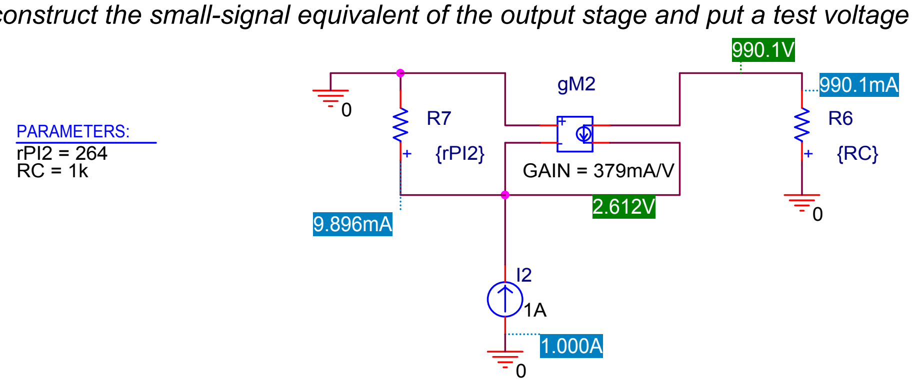

FIGURE 4

Input resistance is $2.612\Omega = r_\pi/(\beta_{ac} + 1)$

[1] For example, C_L could be the C_π of the input transistor of the following stage.

6. Using the open-circuit time constant method, estimate the value of the load capacitance C_L that results in a corner frequency of 4 MHz.

We find the resistances seen by each capacitor, determine the RC time constants, and add them up to find the total time τ. Then $f_C = 1/(2\pi\tau)$. Again, ignore R_B, as it is too large to matter.

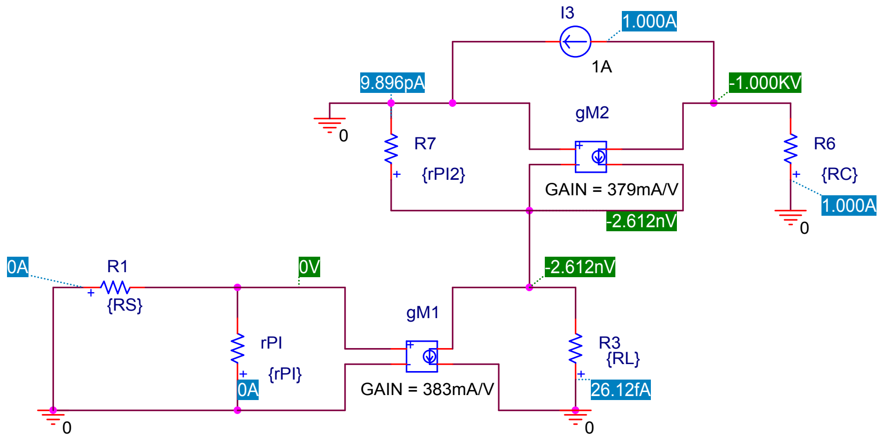

FIGURE 5

For $C_{\mu 2}$ and C_L, R = R_C = 1kΩ

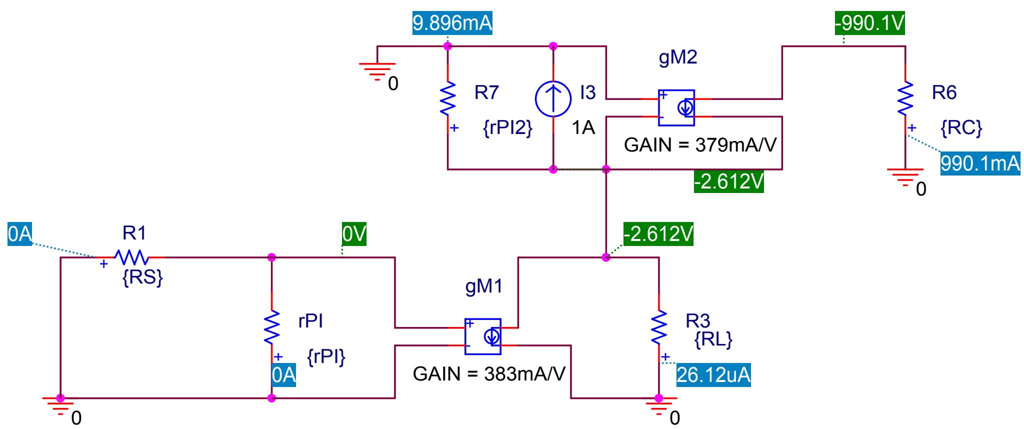

FIGURE 6

For $C_{\pi 2}$, R = r_e = 2.62Ω

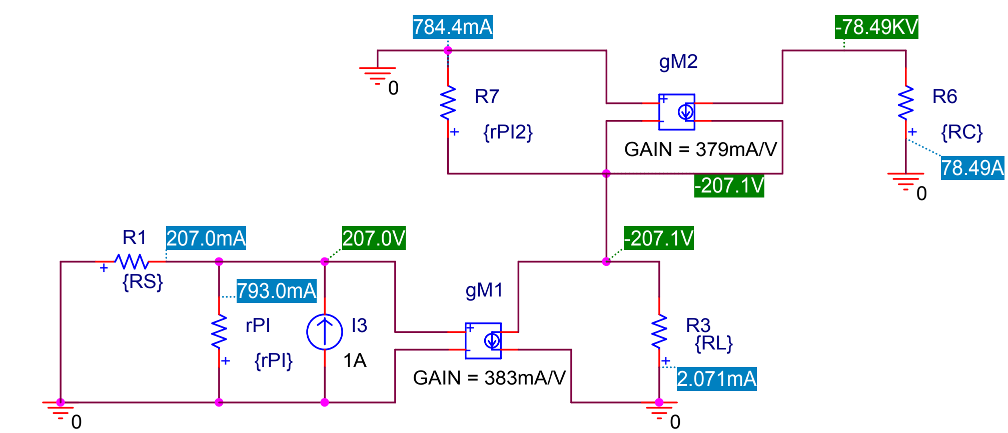

FIGURE 7

For $C_{\pi 1}$, R = $r_{\pi 1}//R_S$ = 207Ω

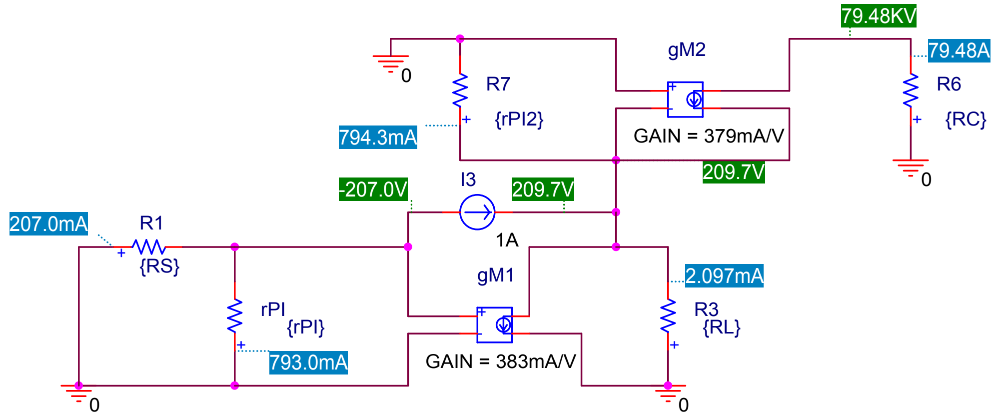

FIGURE 8

For $C_{\mu 1}$, R = $r_{e2} + r_{\pi 1}//R_S + g_{m1}r_{e1}(r_{\pi 1}//R_S)$ = 209.7+207.0 = 416.7Ω

Total time τ *= 5pF(416.7+ 1k)+100pF(207+2.6)+*C_L*1k = 28.04ns+*C_L*1k*

For a corner of 4MHz, require τ *= 1/(2*π *4M) = 39.79 ns =* C_L*1k + 28.04ns →* C_L *= 11.75ns/1k =11.75 pF.*

7. Do you expect your estimate for C_L to be accurate, or too low, or too high? Explain your answer.

The open-circuit method assumes all capacitors are open circuits but the one selected. If in fact some of these capacitors are short-circuits (or, at any rate, not open-circuits), the resistance actually seen by the selected capacitor will be lower than the open-circuit estimate, and the true time constant will be shorter. Therefore, we expect the time constant estimated by the open-circuit method to be an upper bound, and the subtracted amount 28.04 ns to be an upper bound. If the subtracted amount really is lower, C_L *in fact will be larger. So we expect* C_L *= 11.75 ns is a lower bound.*

Problem 2

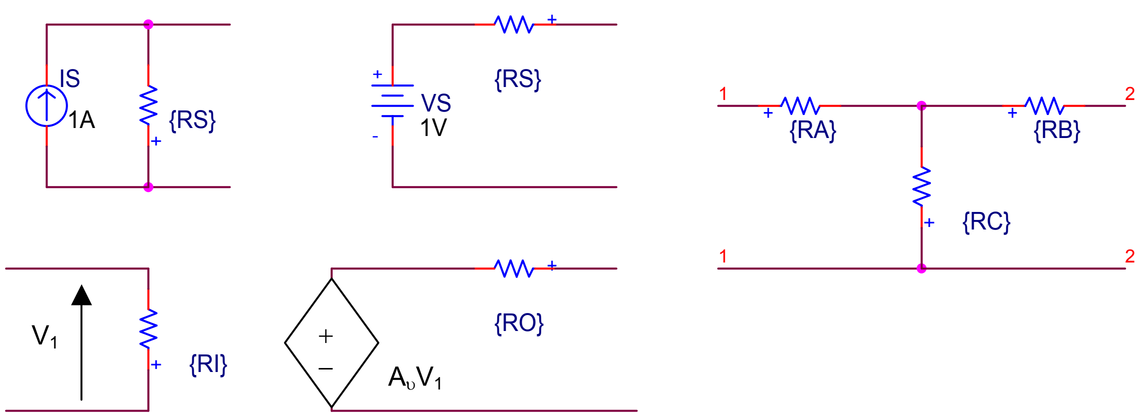

FIGURE 9

Inventory of parts for problem 2; only one of the two signal sources is used

Figure 9 shows two possible signal sources, a T-section feedback network and a voltage amplifier. By following the steps listed below, hook up these parts to make a transresistance amplifier with negative feedback and an overall gain with feedback of 100 V/A.

8. Determine the simplest T-section

We are told that this is a transR amplifier, that is, voltage out and current in. Therefore, β_{FB} *= I/V = VCCS. Therefore, we find the two-port with a VCCS on the left (feedback) side. We find* β_{FB}

$= -- [R_C/(R_C+R_A)]/(R_B+R_A//R_C)$. *If we let* $R_B \to 0$, $\beta_{FB} = --1/R_A$. *Therefore, we need only* R_A *to control* β_{FB}, *and can let* $R_C \to \infty$.

9. Sketch the circuit with the simplified T-section and the <u>appropriate</u> signal source

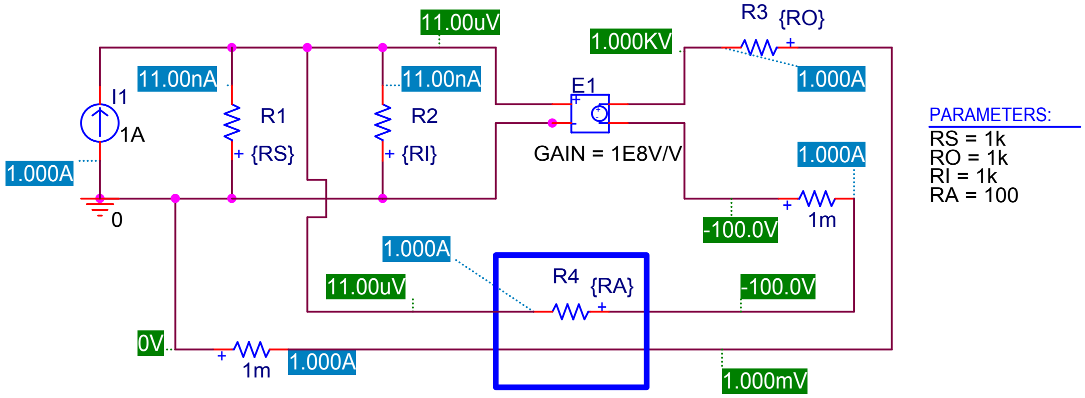

FIGURE 10

Circuit with simplified two-port

10. Show how to determine whether you have negative feedback

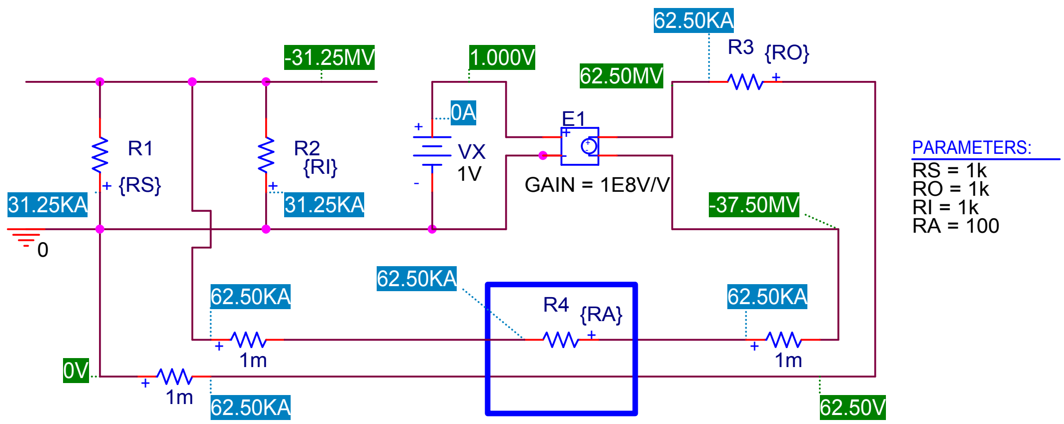

FIGURE 11

Positive test voltage at input shows negative return voltage on input $R_I \to$ negative feedback

11. Find the resistor values for the T-section assuming no loading

For no loading, the closed loop gain is $1/\beta_{FB} = R_A = 100\ V/A \to R_A = 100\Omega$

12. Find the loaded gain with feedback

The loaded gain with feedback is found using the two-port representation of the feedback network and setting $\beta_{FB} = 0$.

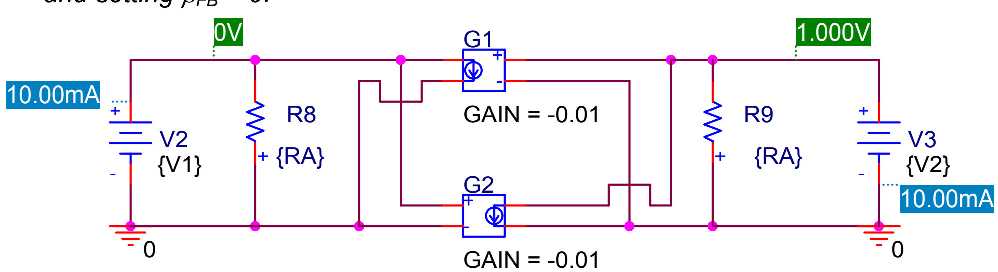

FIGURE 12

Two-port representation of feedback network

Inserting the feedback network, we find $R_A//R_I//R_S$ at the input and $R_O + R_A$ at the output. Consequently the input voltage is $V_I = I_S\,(R_A//R_I//R_S)$ and the output voltage is $V_O = A_\upsilon V_I\, R_A/(R_A + R_O) = I_S\,(R_A//R_I//R_S)\, A_\upsilon\, R_A/(R_A + R_O) \rightarrow V_O/I_S = (R_A//R_I//R_S)\, A_\upsilon\, R_A/(R_A + R_O)$. The loaded gain with feedback is then

$$A_\upsilon(FB) = (R_A//R_I//R_S)\, A_\upsilon\;\, R_A/(R_A + R_O)/\{1+\beta_{FB}(R_A//R_I//R_S)\, A_\upsilon\;\, R_A/(R_A + R_O)\}$$
$$= \;(R_A//R_I//R_S)\, A_\upsilon\;\, R_A/(R_A + R_O)/\{1+ (R_A//R_I//R_S)\, A_\upsilon\;\, /(R_A + R_O)\}$$

Problem 3

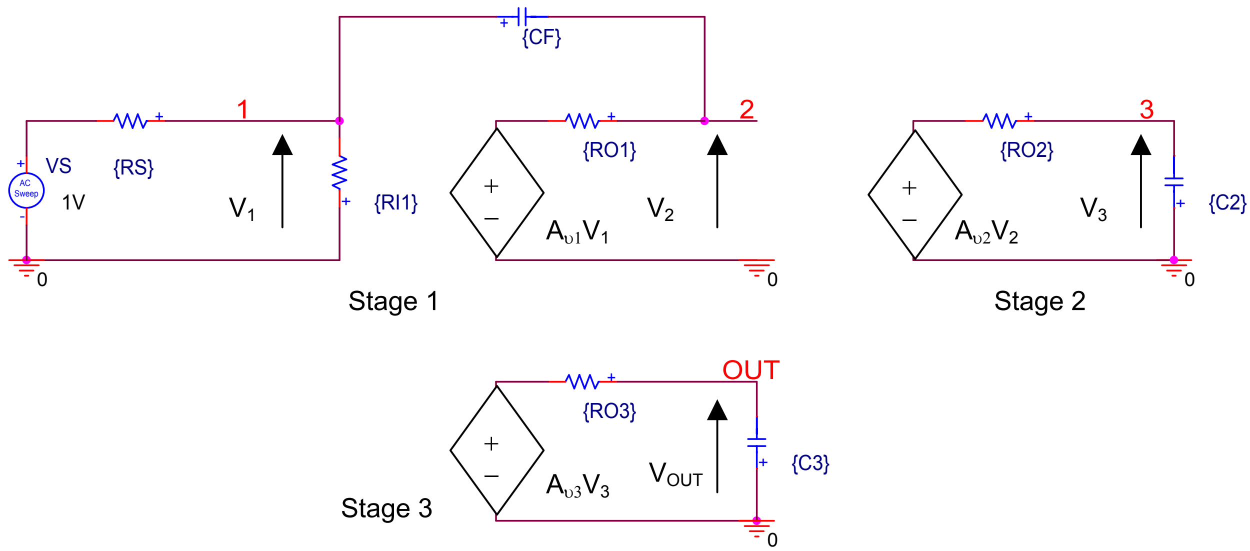

FIGURE 13

Three-stage amplifier for Problem 3

Using the three-stage amplifier of Figure 13, do the following.

1. Find formulas for the pole frequencies f_1, f_2, ... in Hz using the open-circuit time-constant method

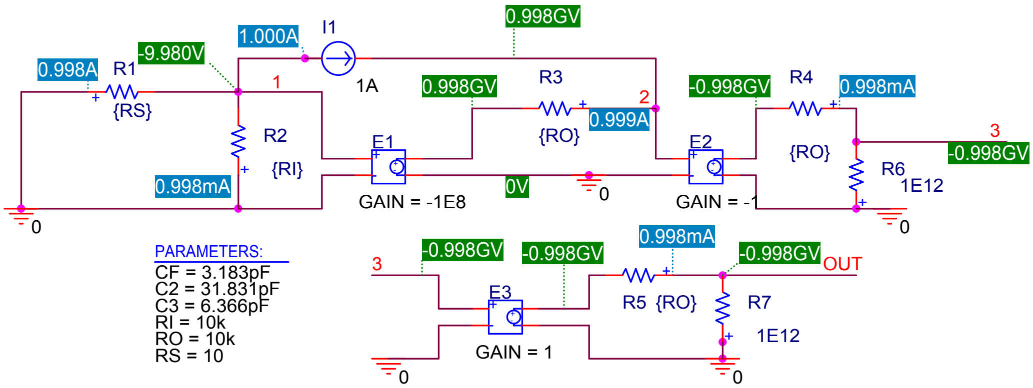

FIGURE 14

For C_F, R = 0.998 GΩ; $f_1 = 1/(2\pi RC_F) = 1/(2\pi\ 0.998 \times 3.183 \times 10^{9-12}) = 50.1$ Hz.

$R = R_{O1}+(1-A_\upsilon)(R_S//R_I) = 10k + 1E8 * 9.99 = 9.99E8$; PSPICE does not satisfy KCL. Error is negligible.

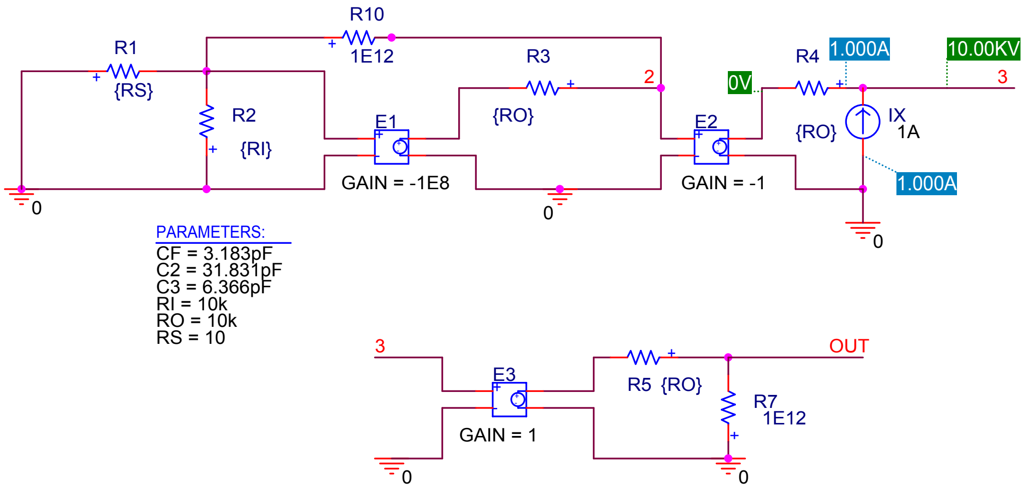

FIGURE 15

For C_2, $R = R_O = 10\ k\Omega$; $f_2 = 1/(2\pi C_2 R) = 1/(2\pi \times 31.831p \times 10k) = 500\ kHz$

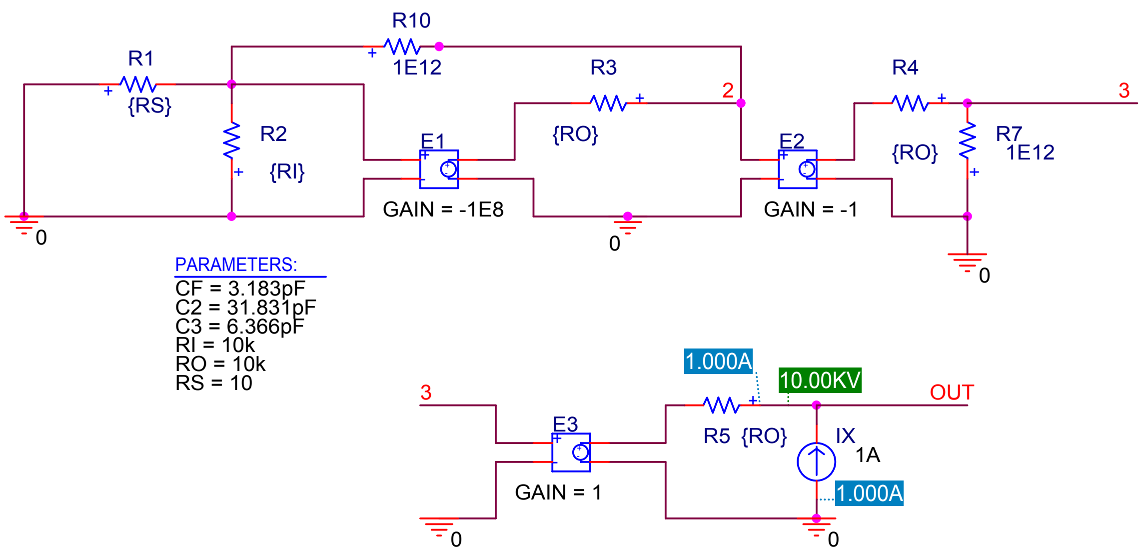

FIGURE 16

For C_3, $R = R_O = 10\ k\Omega$, $f_3 = 1/(2\pi C_3 R_O) = 1/(2\pi\ 6.366pF \times 10k) = 2.5\ MHz$

2. Find a formula for the voltage gain V_{OUT}/V_S at zero frequency (DC)

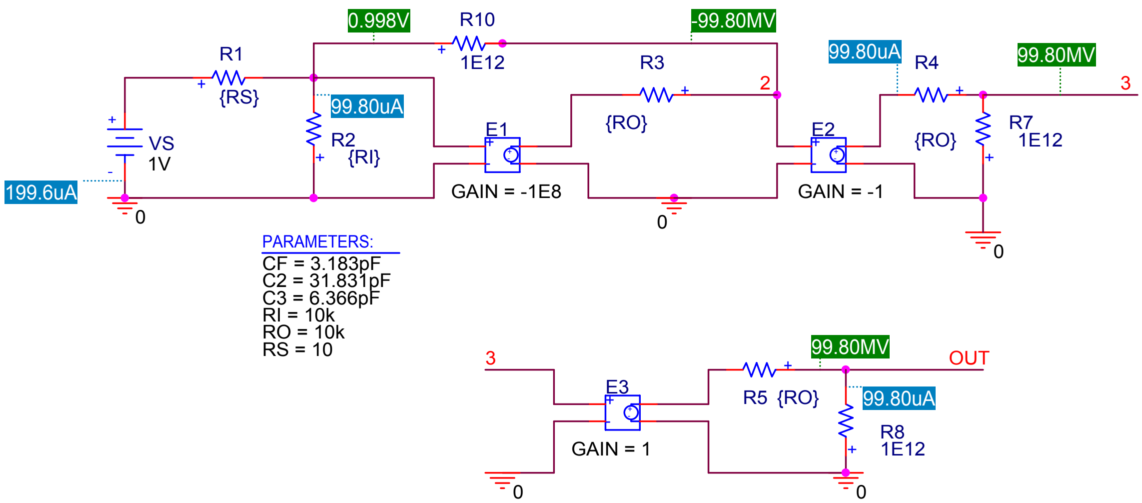

FIGURE 17
Voltage gain at zero frequency

$$Gain = A_{\upsilon 3}A_{\upsilon 2}A_{\upsilon 1}R_I/(R_I + R_S) = 10^8 \text{ x } 10^4 / (1+ 10^4) = 99.99 \text{ x } 10^6 \text{ V/V}$$

3. Find a formula for the voltage gain including frequency dependence and put it in standard form as a product of zeros, high-pass and low-pass factors in standard form. Use the notation f_1, f_2, ... for the pole frequencies in Hz

$$Gain = A_{\upsilon 3}A_{\upsilon 2}A_{\upsilon 1}R_I/(R_I + R_S) \text{ x } \{(1+jf/f_1)(1+jf/f_2)(1+jf/f_3)\}^{-1}$$

4. Make Bode phase and dB magnitude plots for the case in Figure 18 with gains given by $A_{\upsilon 1} = -10^8$ V/V, $A_{\upsilon 2} = -1$ V/V, $A_{\upsilon 3} = 1$ V/V. Label all corners (frequency and value) and slopes. On both plots indicate the number of decades in frequency between breaks in the curves. Use numerical values in Hz for frequencies, <u>not</u> radians.

PARAMETERS:
CF = 3.183pF
C2 = 31.831pF
C3 = 6.366pF

RO1 = 10k
RO2 = 10k
RO3 = 10k

RS = 10
RI1 = 10k

FIGURE 18
Parameter values for Bode plots

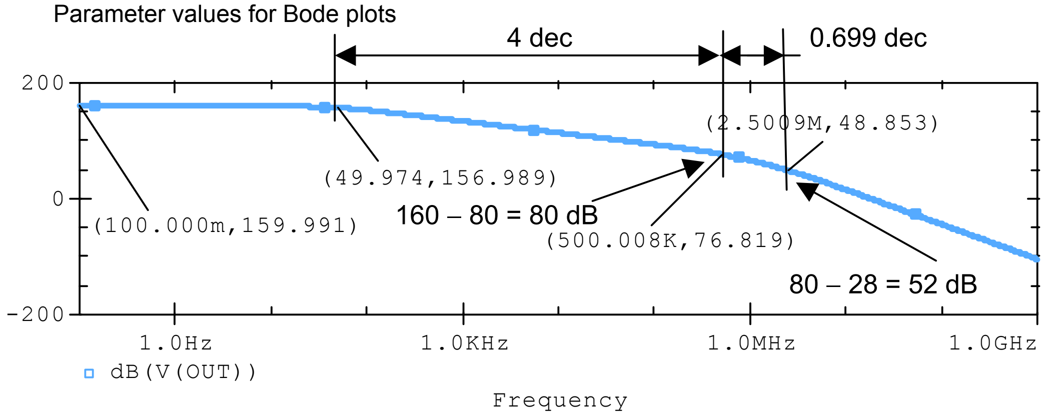

FIGURE 19
Bode magnitude plot

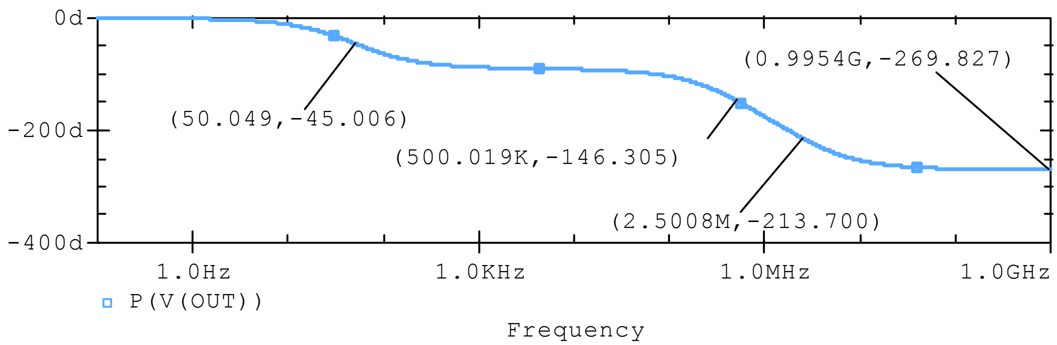

FIGURE 20

Bode phase plot – approximation of widely spaced poles would make ϕ(500kHz) = –135° and ϕ(2.5MHz) = –225°

5. Assuming this amplifier is used to make a feedback voltage amplifier, find the maximum value of feedback β_{FB} in units of V/V that allows a 45° phase margin

For a phase margin of 45°, ϕ = –135°. Using Bode plots assuming widely spaced poles, we'd expect –135° at location of second pole, setting f_{135} = 500 kHz. At this frequency the Bode gain plot shows A_υ = 80dB = 10^4V/V → $\beta_{FB} = 1/10^4 = 10^{-4}$V/V

6. Assuming the approximation of widely spaced poles, describe a method to select C_F so the phase margin of a feedback voltage amplifier based on Part 4 is 45° at a specified value of β_{FB}.

Method: Draw line on Bode magnitude plot at $1/\beta_{FB}$ and find point on this curve corresponding to location of second pole. Draw a line at 20 dB/decade backward from this point to the zero frequency gain value. This intersection is the new pole frequency. Find ratio 'r' of original frequency of lowest pole to this new frequency; $r = f_{ORIG}/f_{NEW}$. This is the ratio of the new capacitance value to the original capacitance value. Then $C_{NEW} = C_{ORIG} \times r$.

7. Using the method of Part 6, for the amplifier of Part 4 show your calculation of the value for C_F for a 45° phase margin with $\beta_{FB} = 10^{-2}$ V/V.

Value of $1/\beta_{FB}$ = 100 → 40 dB. This value is 120dB down from zero f gain. At 20 dB/dec, it takes 6 dec to rise to zero f gain of 160 dB, so new lowest pole has to be $f_{P2}/10^6 = 500k/10^6 = 0.5$Hz. The original lowest pole frequency is 50Hz, so the reduction in frequency is a factor of 10^2, suggesting that $C_{NEW} = 100C_{ORIG} = 100 \times 3.183$pF = 318.3pF.

8. What is the actual (not approximate) phase margin using your new value for C_F?

At $1/\beta_{FB}$ = 40 dB, the unity gain frequency is f_1 = 500 kHz; at this frequency the phase is

$$\phi = -\{\tan^{-1}(f_1/f_{P1}) + \tan^{-1}(f_1/f_{P2}) + \tan^{-1}(f_1/f_{P3})\}$$
$$\approx -\{90° + 45° + \tan^{-1}(500k/2.5M)\} = -135° - 11.3° = -146.3°$$

Therefore, the phase margin is $\phi_M = -146.3° + 180° = 33.7°$.