

### ECE 304: Final Exam Spring '05

NOTE: IN ALL CASES

1. Solve the problem on scratch paper
2. Once you understand your solution, put your answer on the answer sheet
3. Follow your answer with an outline of your solution. No points for answer without an outline of the solution. A mish-mash of computation is not an acceptable outline.

PRINT your name at the top of each answer sheet

Assume in all problems  $V_{TH} = 25.864 \text{ mV}$ , and  $V_{BE} = V_{TH} \ln\{I_C(V_{CB}=0V)/I_S\}$

#### Problem 1: Cascode

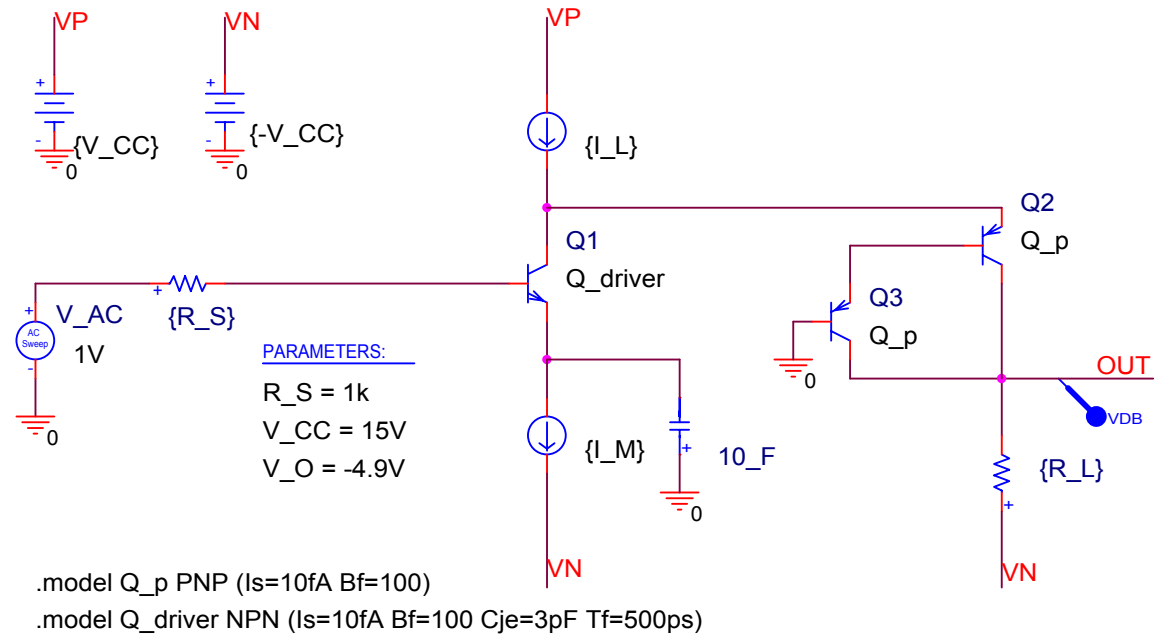


FIGURE 1

Cascode amplifier; all Early voltages are infinite

Assume  $R_S = 1 \text{ k}\Omega$  and the output voltage is  $V_O = -4.9V$ . Notice that only the driver transistor has capacitance, and that is due to  $C_\pi$ . Capacitance  $C_\pi$  satisfies EQ. 1 below with  $C_{JE} = 3 \text{ pF}$ ,  $T_F = 500 \text{ ps}$ ,  $I_C =$  collector current of Q1.

EQ. 1 
$$C_\pi = C_{je} + \frac{I_C \tau_F}{V_{TH}}$$

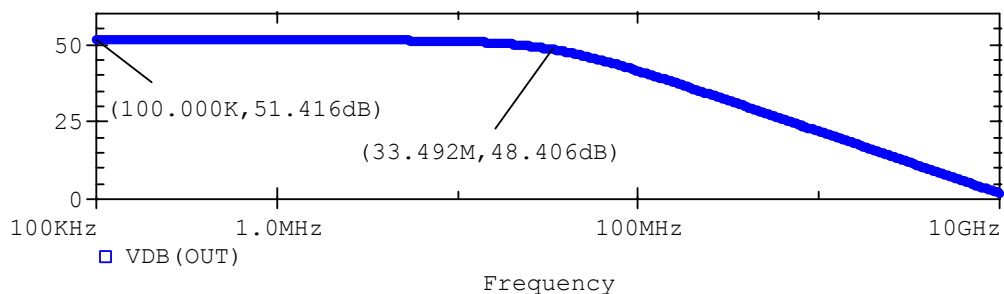
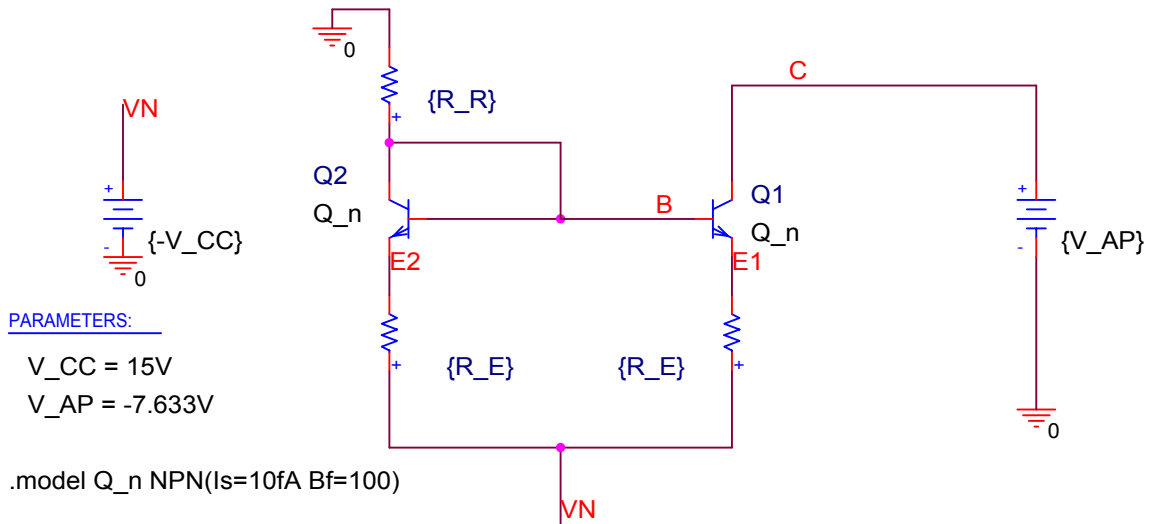


FIGURE 2

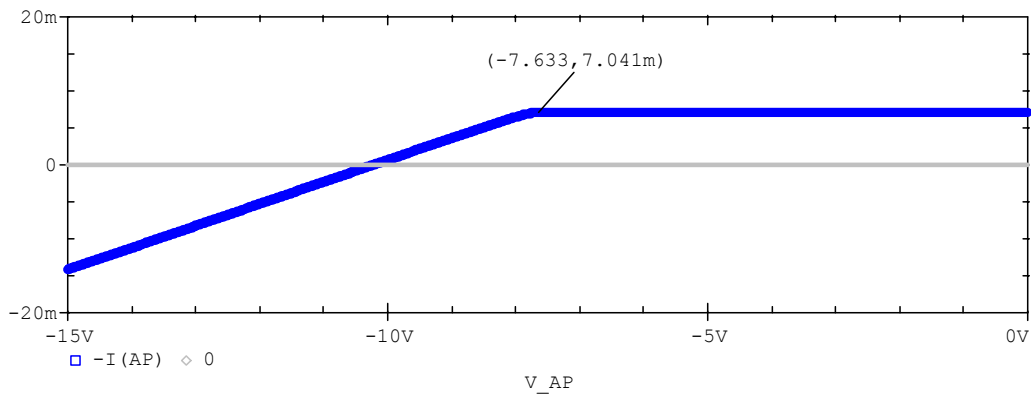
Small-signal gain of 51.416 dB and corner frequency of 33.492 MHz

1. Select the current sources  $I_L$  and  $I_M$ , and the load  $R_L$  so the amplifier of Figure 1 has the small-signal gain behavior shown in Figure 2.
2. If  $C_\mu \approx 3 \text{ pF}$  were added to Q1, how much would it affect the bandwidth? Be quantitative.

**Problem 2: Current Mirror**



**FIGURE 3**  
 Current mirror; all Early voltages are infinite

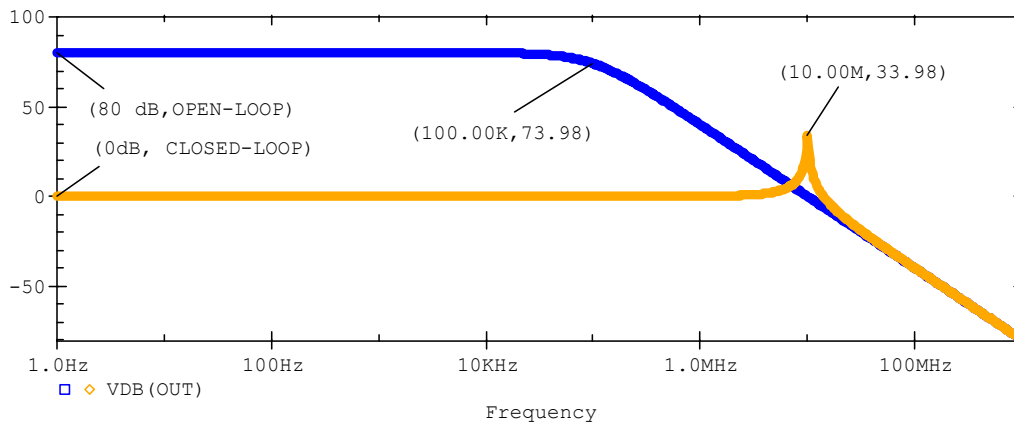


**FIGURE 4**  
 DC current-voltage behavior of mirror; mirror current is 7.041 mA at  $V_{AP} = -7.633 V$

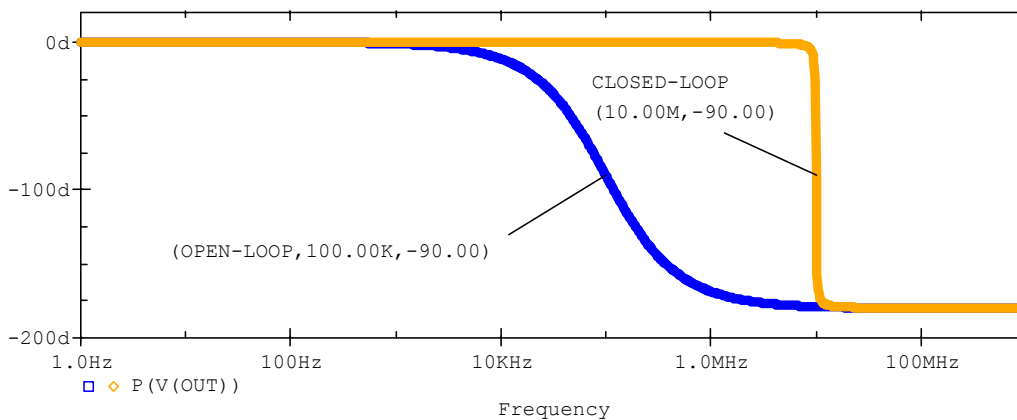
1. Select  $R_R$  and  $R_E$  so the mirror in Figure 3 has the behavior shown in Figure 4. That is, current is 7.041 mA for  $V_{AP} \geq -7.633 V$ . Check that your design satisfies these specs. Assume forward bias of the CB junction in saturation is  $V_{CB} = -450 mV$ .
2. Based upon circuit operation (that is, *not* just estimating numbers from Figure 4), derive a formula for the slope of the  $I$ - $V$  curve in the region  $V_{AP} < -7.633 V$  including discussion of mode assignments to the transistors

*Hint for Part 2:* Assume that base-emitter voltages don't change much with  $V_{AP}$ .

**Problem 3: Compensation**



**FIGURE 5**  
Bode magnitude plot for open- and closed-loop amplifier

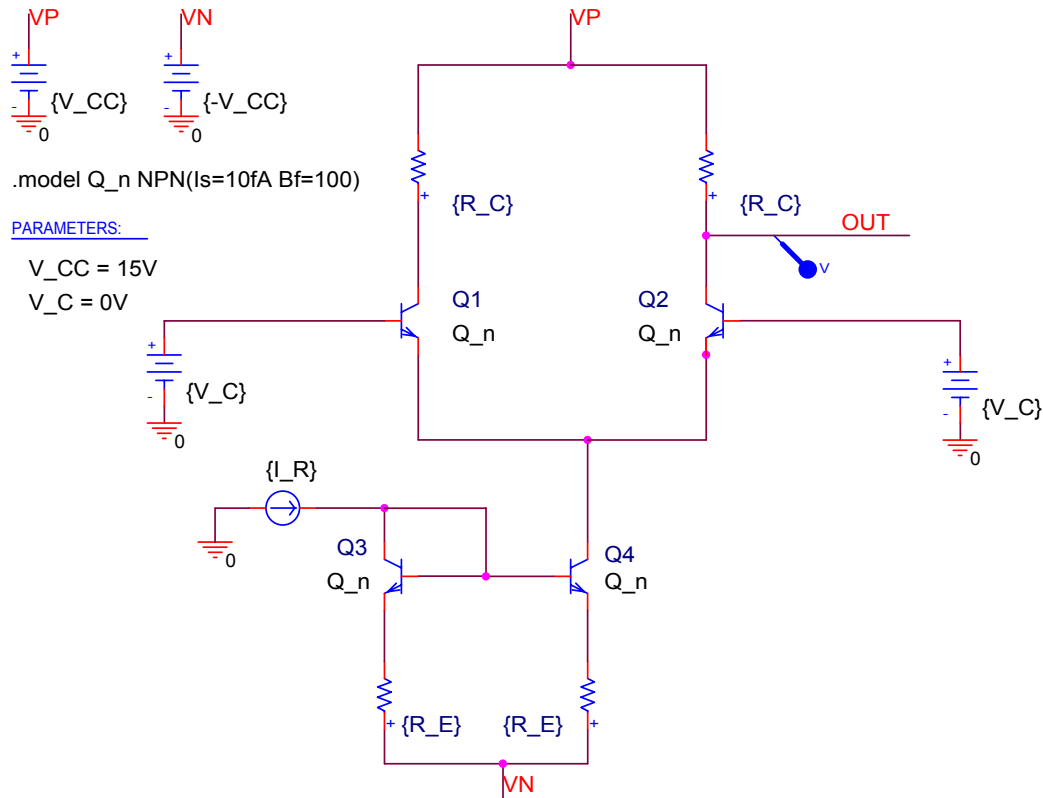


**FIGURE 6**  
Bode phase plot for open- and closed-loop amplifier

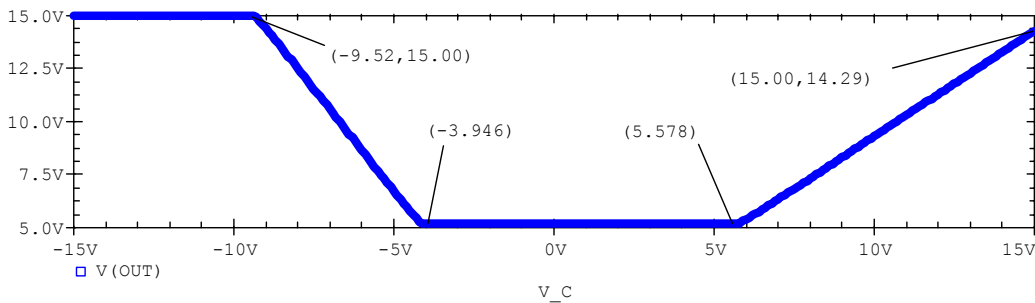
We have an amplifier with open-loop Bode plots shown in Figure 5 and Figure 6. Also shown are closed-loop Bode plots for the case of unity feedback ( $\beta_{FB} = 1 \text{ V/V}$ ).

1. Find a formula for the open-loop gain as a function of frequency in Hz.
2. Find the phase margin of the closed-loop amplifier shown.
3. Compensate this amplifier by adding a pole so the gain drops 20 dB/dec down to 0 dB at the next pole. Find the frequency needed for the added pole.
4. Sketch Bode phase and magnitude plots for the open-loop amplifier with the added pole present. Label the phase at 0 dB, and label all slopes and corners.
5. Find the two-pole amplifier that approximates the compensated amplifier. Will the compensated amplifier exhibit good step response? Why or why not?
6. Change the compensation to obtain a phase margin at 0dB of  $45^\circ$ . What is the revised pole frequency?
7. Sketch the Bode plots for the open-loop amplifier with the revised pole position. Label the phase at 0 dB, and label all slopes and corners.
8. Will this revised compensated amplifier exhibit good step response? Why or why not?

#### 4. Differential amplifier



**FIGURE 7**  
Differential amplifier; all Early voltages are infinite



**FIGURE 8**  
Common-mode transfer characteristic

Assume  $R_C = 1 \text{ k}\Omega$  and assume maximum reverse bias of CB junction in saturation is  $V_{CB} = -385 \text{ mV}$ .

1. Select  $I_R$  and  $R_E$  so the amplifier has the common mode range seen in Figure 8.

The transfer characteristic in Figure 8 exhibits four ranges, from right to left:

Range 1:  $V_C > 5.578 \text{ V}$ , Range 2:  $-3.946 \text{ V} < V_C < 5.578 \text{ V}$ ,  
Range 3:  $-9.52 \text{ V} < V_C < -3.946 \text{ V}$ , and Range 4:  $V_C < -9.52 \text{ V}$ .

2. List the ranges in a vertical column, and tabulate the modes of all transistors in each range.
3. Based upon circuit operation (that is, *not* just estimating numbers from Figure 8), derive a formula for the slope of the transfer characteristic in each range.