ECE 304 Spring '06: Lab 2
Current Mirror Design Project

Objective

To make a current mirror design tool and test one of its designs by building it.

Schematic

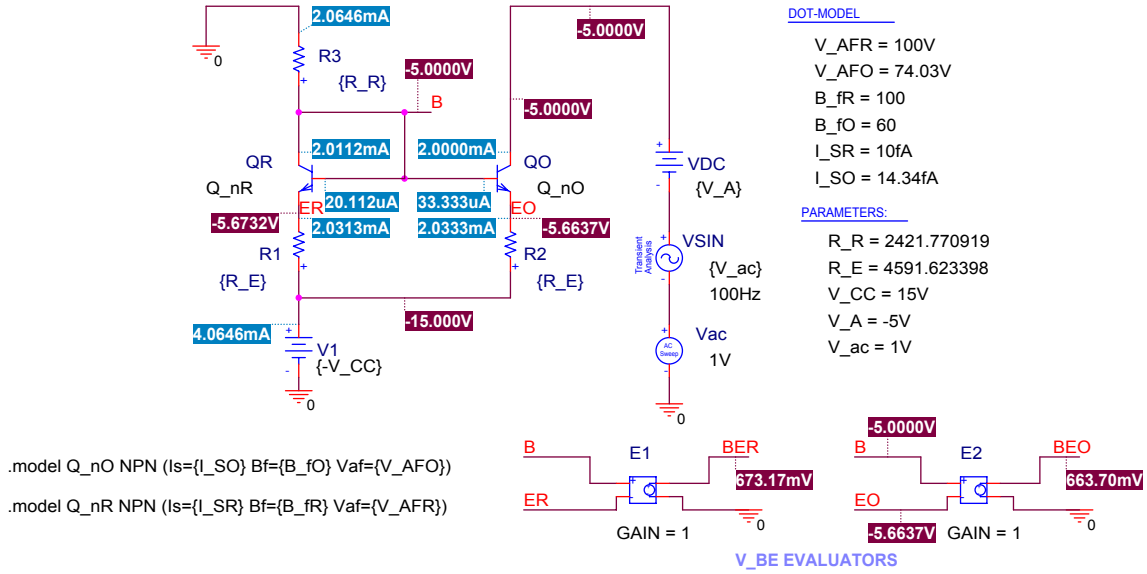

FIGURE 1

Schematic for current mirror with mismatched transistors

Figure 1 shows the circuit schematic and dot-model statements (repeated below for easy copying). At the bottom of the schematic are two evaluator circuits that have nothing to do with the current mirror operation, but display the base-emitter voltages for comparison with the spreadsheet. The evaluators make it unnecessary to mentally subtract two voltages on the schematic itself.

Dot-model statements

```
.model Q_nR NPN (Is={I_SR} Bf={B_FR} Vaf={V_AFR})
.model Q_nO NPN (Is={I_SO} Bf={B_FO} Vaf={V_AFO})
```

FIGURE 2

Dot-model statements for ideal mismatched transistors; you will use the parameters you measured for your Q2N2222 transistors

Specifications

The specifications could involve any of the following properties, illustrated with the example of Figure 1.

1. A maximum output voltage swing that the mirror will be subjected to, say V_{ac}. Under these conditions, the output current from a transient simulation using a sinusoidal output voltage superposed on the DC background is shown in Figure 3. The upward blip in current shows that the mirror is on the edge of going into the low Norton resistance region at this AC voltage. The upward spike increases rapidly as V_{ac} is increased.

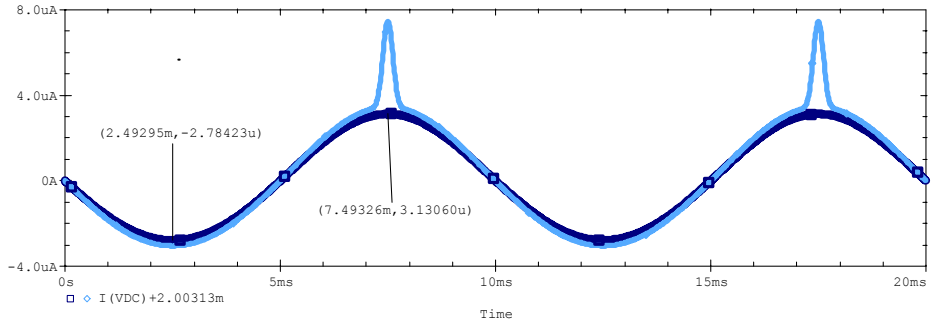

FIGURE 3

Transient mirror current for set-up of Figure 1 for V_{ac} = 5 V and 5.5 V, and V_A = 0 V

2. A DC current level the mirror produces when $V_A = V_B$. Figure 1 produces about 2 mA for voltages above the compliance voltage.
3. A compliance voltage V_{CV} that specifies how low the DC voltage across the mirror can be and still have a DC output current of I_O. In Figure 4 we see the mirror of Figure 1 has a compliance voltage of about V_{CV} = –5 V.

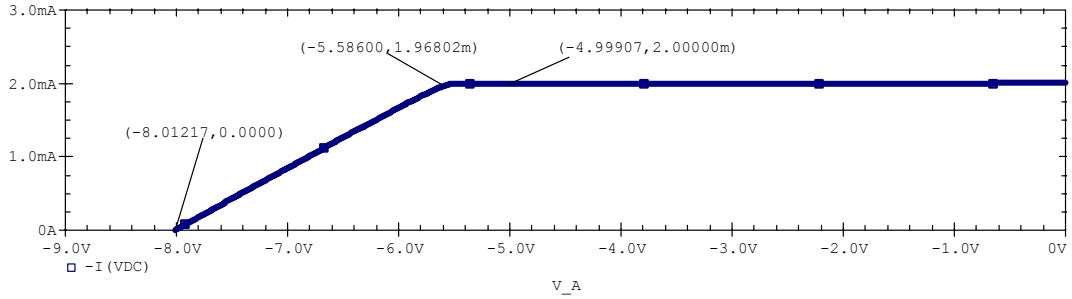

FIGURE 4

DC I-V plot for mirror of Figure 1 showing delivered DC output current of I_O =2 mA for V_A = V_B = -5V; the compliance voltage is slightly lower at V_{CV} = -5.58 V

4. A maximum AC ripple current that should result when the maximum swing is present, V_{ac}/R_N, where R_N is the small-signal mirror resistance. Figure 3 shows the ripple as 3 μA for a 5 V swing. Figure 5 shows that R_N increases as R_E increases until, at R_E = 4.9 kΩ the output transistor saturates forcing the mirror into the low resistance regime, where R_N drops abruptly. As long as R_N increases with R_E, the AC ripple current V_{ac}/R_N will drop as R_E is increased.

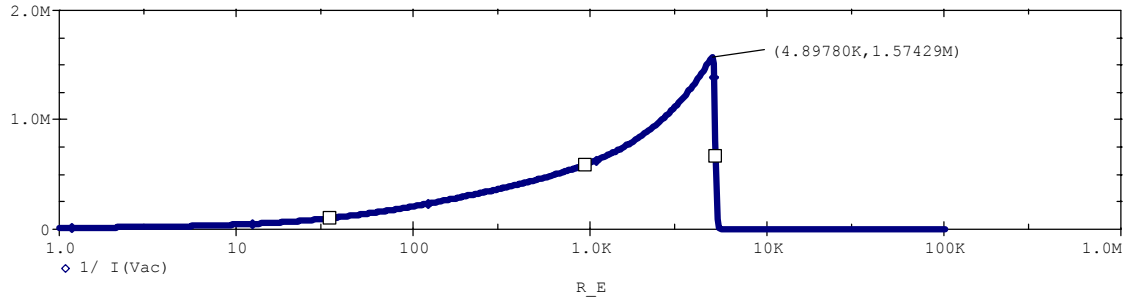

FIGURE 5

Dependence of mirror Norton resistance R_N upon value of leg resistor R_E for mirror of Figure 1

The specifications 1-4 above are interconnected, and only two independent requirements can be specified, because the mirror has only two independent parameters, R_E and R_R. For example,

specification of the DC mirror current at a specified applied voltage and simultaneous specification of the compliance voltage are sufficient to determine the design,.

Design Tool

The design tool consists of a spreadsheet based upon formulas of a hand analysis and verified by PSPICE simulations. The organization of the spreadsheet is shown in Figure 6.

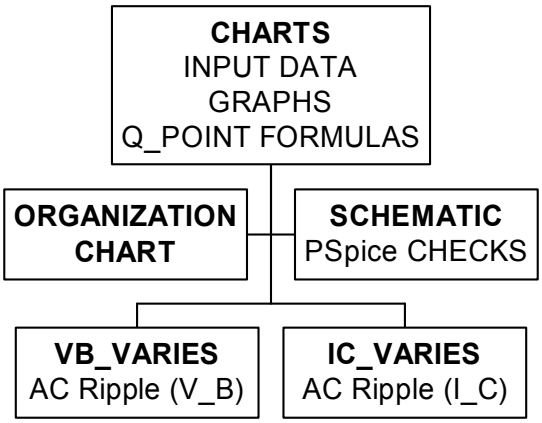

FIGURE 6
Organization of the worksheets in the spreadsheet

This flow chart is inserted on the worksheet ORGANIZATION using the menu INSERT/OBJECT and selecting MS ORGANIZATION CHART, as shown in Figure 7.

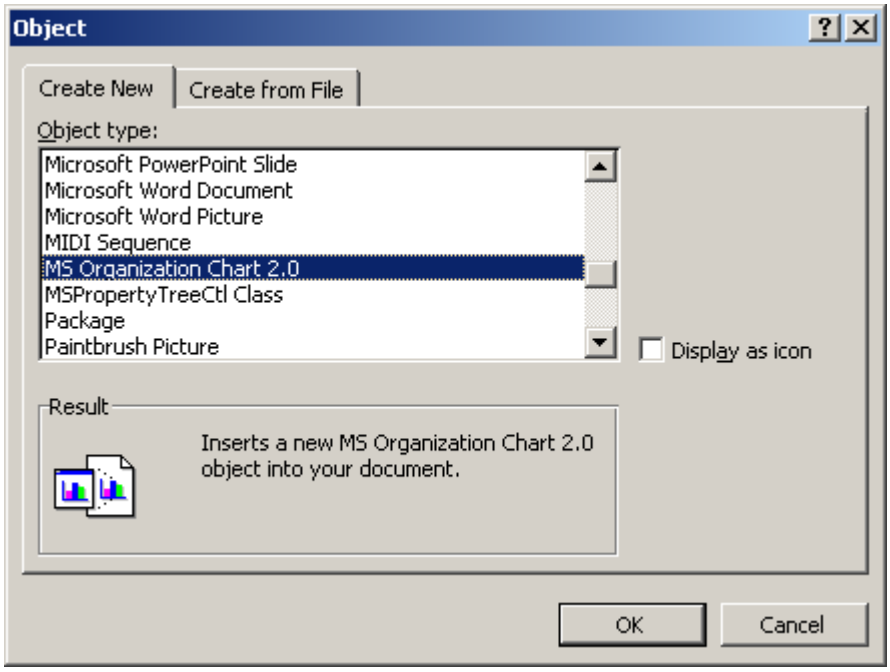

FIGURE 7
Inserting a flowchart into EXCEL

The other worksheets are shown below. Cells F8 and F9 on the CHARTS worksheet of Figure 8 below show that the base voltage V_B and the output current I_C in mA for $V_A = V_B$ are chosen as the design variables. These two variables are chosen because they make the formulas simple for the rest of the design. The circuit design requires values for the resistors R_E and R_R, which are conveniently copied from the calculations into the DESIGN SUMMARY box. Regardless of which two

independent mirror properties from the previous list are specified, the spreadsheet enables selection of values of R_E and R_R that will meet the specifications.

	C	D	E	F	G
3				Design Summary	
4			Ω	R_R	2421.77092
5	**CHARTS Worksheet**		Ω	R_E	4591.6234
6	Design assumes V_A = V_B				
7					
8	Input	Base voltage	V	V_B	-5
9		Mirror current @ V_A=V_B	mA	I_C(mA)	2
10		AC input voltage amplitude	V	V_AC	1
11		Supply voltage	V	V_CC	15
12		Thermal voltage	V	V_TH	0.025864
13					
14	Dot-Model	Early voltage (ref)	V	V_AFR	100
15		Early voltage (out)	V	V_AFO	74.03
16		DC beta @V_CB=0 (ref)		B_DCR	100
17		DC beta @ V_CB=0 (out)	A/A	B_DCO	60
18		AC beta @V_CB=0 (ref)	A/A	B_ACR	100
19		AC beta @ V_CB=0 (out)	A/A	B_ACO	60
20		Scale current (ref)	A	I_SR	1.000E-14
21		Scale current (out)	A	I_SO	1.434E-14
22					
23	Calculated	Change units	A	I_C	0.002
24		Output emitter-base V	V	**V_BEO**	0.66369909
25		Leg resistor	Ω	R_E	4591.6234
26	Iteration	Initial guess	V	V_BER1	0.7
27	for			I_CR1	0.00200537
28	I_CR			V_BER2	0.67309163
29	and			I_CR2	0.00201118
30	V_BER			V_BER3	0.67316635
31				I_CR3	0.00201116
32				V_BER4	0.67316615
33				I_CR4	0.00201116
34				V_BER5	0.67316615
35				I_CR5	0.00201116
36		Emitter-base V		**V_BER**	0.67316615
37		Ref Transistor IC		I_CR	0.00201116
38		Reference resistor	Ω	R_R	2421.77092
39					
40	AC	NPN base resistance	Ω	**r_PIR**	1286.02403
41	ripple	NPN base resistance	Ω	**r_PIO**	775.92
42	current	Emitter current (ref)	A	I_ER	0.00203127
43	for	NPN ref emitter resistance	Ω	r_ER	12.7329112
44	V_ac	R_R//(r_ER+R_E)	Ω	R_EFF	1587.03306
45	sine	NPN output resistance	Ω	**r_O**	37015
46	wave	Small-signal mirror R	Ω	R_N	1.507E+06
47	at output	Output current ripple	μA	I_AC(uA)	0.66362959
48					
49	Cross	Leg resistor (ref)	Ω	R_E	4591.6234
50	check	Compare with output side value		% Error	1.9808E-14

FIGURE 8

Layout of CHARTS worksheet including hand analysis formulas for the mirror at $V_A = V_B$, that is, for the case where $V_{CB} = 0$ V for both transistors

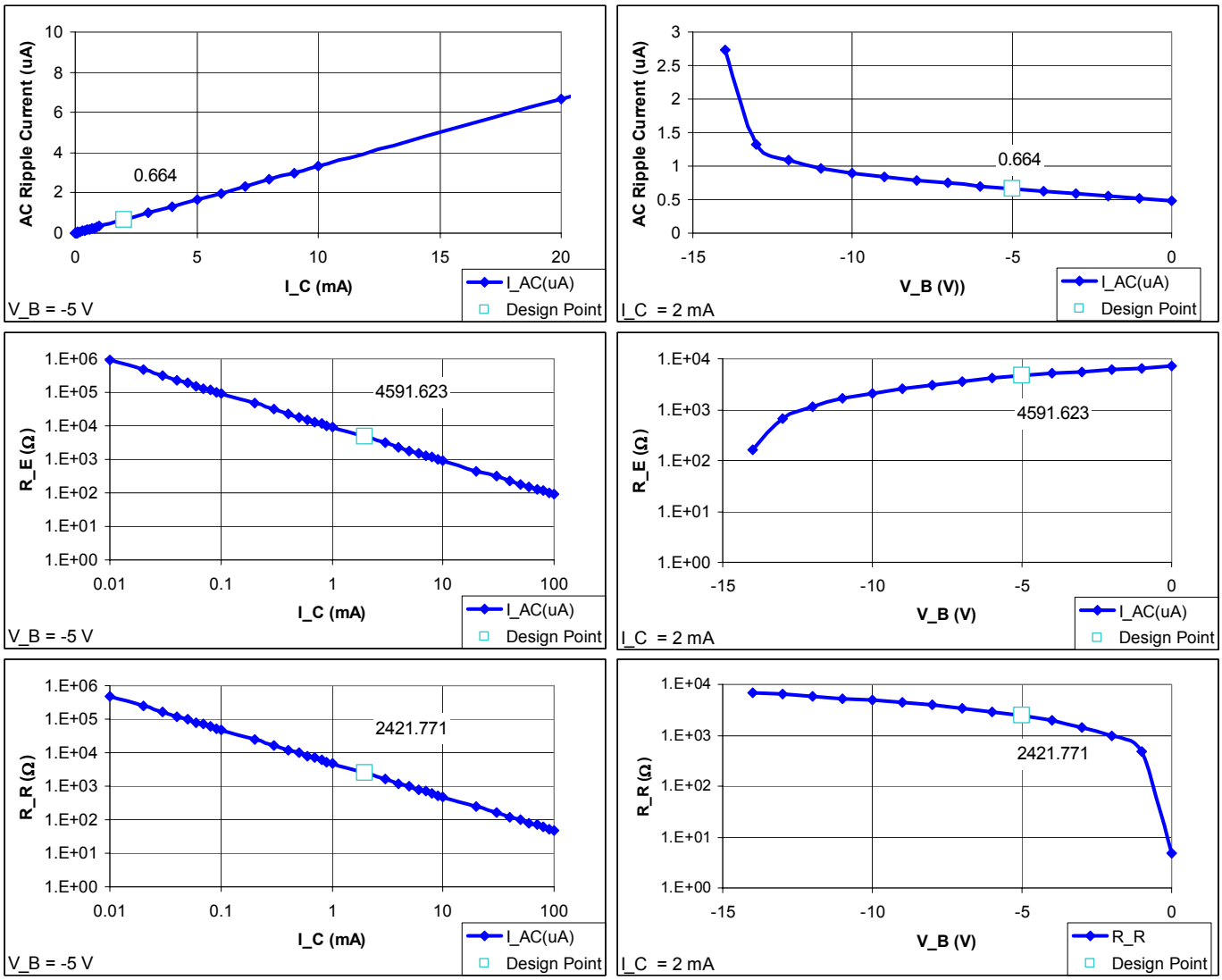

FIGURE 9

Charts on the CHART worksheet; the calculations are done on worksheets IC_VARIES and VB_VARIES

I_CR1 = =(V_CC+V_B-V_BER1)/(R_E*(1+1/B_DCR))

	C	D	E	F	T	U	V	W	X	Y	Z	AA	AB	AC	AD	AE	AF
5	IC_VARIES Worksheet																
6	Label	V_B = -5 V															
7																	
8			V_B	I_C(mA)	I_C	V_BEO	R_E	V_BER1	I_CR1	V_BER2	I_CR2	V_BER3	I_CR3	V_BER4	I_CR4	V_BER5	I_CR5
9			-5	0.01	0.00001	0.526663	931803.6	0.7	9.88E-06	0.535679	1.01E-05	0.536132	1.01E-05	0.536131	1.01E-05	0.536131	1.01E-05
10				0.02	0.00002	0.544591	465020.1	0.7	1.98E-05	0.553656	2.01E-05	0.554059	2.01E-05	0.554058	2.01E-05	0.554058	2.01E-05
11				0.03	0.00003	0.555078	309669.6	0.7	2.97E-05	0.564171	3.02E-05	0.564546	3.02E-05	0.564545	3.02E-05	0.564545	3.02E-05
27				1	0.001	0.645772	9200.88	0.7	0.001001	0.655114	0.001006	0.655239	0.001006	0.655239	0.001006	0.655239	0.001006
28				2	0.002	0.663699	4591.623	0.7	0.002005	0.673092	0.002011	0.673166	0.002011	0.673166	0.002011	0.673166	0.002011
29				3	0.003	0.674186	3057.644	0.7	0.003011	0.683608	0.003017	0.683653	0.003017	0.683653	0.003017	0.683653	0.003017
30				4	0.004	0.681627	2291.403	0.7	0.004018	0.691069	0.004022	0.691094	0.004022	0.691094	0.004022	0.691094	0.004022

IC_Varies | VB_Varies

FIGURE 10

Segment of IC_VARIES worksheet; first iteration for I_CR is in FORMULA BOX

The IC_VARIES worksheet is formed by copying columns F and G on CHARTS and using menu PASTE SPECIAL/TRANSPOSE to paste these columns as rows on a new worksheet. Then a column of values is entered for the variable to be varied, I_C in this case, and this column is named using INSERT/NAME/CREATE. Then the calculated variable formulas are filled in under their column

headings using the cursor. The cursor is dragged to the corner of the cell until it becomes a plus sign, and then it is dragged down the column holding down the left mouse button, as shown in Figure 11 below.

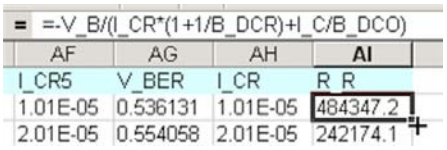

FIGURE 11
Using the cursor to fill in a column of formulas, in this case R_R

All the columns can be done at once. However, only the CALCULATED variables should be filled in. Columns T to AR are named using INSERT/NAME/CREATE. COLUMN AT is not named, because that would conflict with COLUMN V. COLUMNS F to R are not filled in and are not named, because we want the input data values to come from the entries on worksheet CHARTS, and do not want them replaced by values on this worksheet.

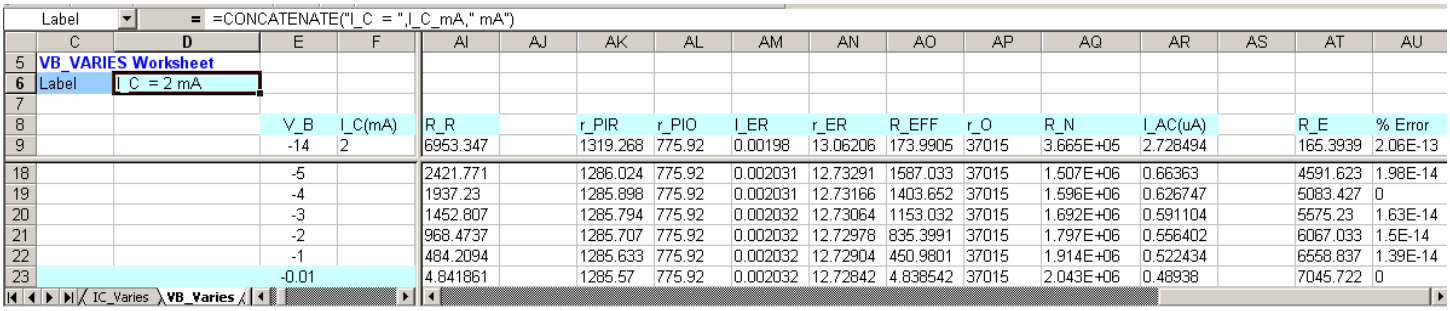

FIGURE 12
Segment of VB_VARIES worksheet, made the same way as IC_VARIES; the CONCATENATE function is used to make a label for the lower left corner of the charts, as seen in Figure 9

Discussion

The transistor parameters are labeled with R for reference transistor and O for output transistor. The spreadsheet is set up with equations based on ideal transistors. Example dot-model statements for such transistors are shown in Figure 2, and these transistors are used to verify the spreadsheet by checking against PSPICE.

Verification of spreadsheet

The spreadsheet is verified by running a schematic at the Q-point and comparing with the spreadsheet Q_point currents and voltages and also by running curves like Figure 4 and Figure 5 and using a table to compare several points on each PSPICE curve with the spreadsheet.

Specifications

Using your Q2N2222 transistor parameters, design a mirror using your EXCEL tool to meet these specifications:

- Supply voltage is V_{CC} = 6 V.
- Resistor values for R_E are nominal 10% values. Actual values can vary from 10% above to 10% below nominal value and circuit still will meet specs. R_R is a pot.
- Lowest DC output current at $V_{CB}(Qo)$ = 0V is I_O = 10 mA.
- Worst case AC ripple current is 37 µA for 4.5 V AC swing.
- Choose the most favorable placement of transistors; for example, maybe it is best to put your highest β or your highest V_{AF} transistor as the output transistor. Use the spreadsheet to find the best arrangement.
- Determine the best V_{CV} for the mirror. Assume $V_{CV} = V_B - 0.5V$ and find best V_B.
- Spreadsheet verification is as in the section VERIFICATION OF SPREADSHEET

Prelab

1. Derive the equations needed for the spreadsheet using mismatched transistors.
2. Set up the spreadsheet and test it. Paste figures like those shown here in your lab notebook.
3. Tabulations of the comparisons between spreadsheet and PSPICE should be provided for bias point currents and voltages (for example, V_{BE}-values and I_C values) and small-signal parameters (r_π's and r_O's and β's from OUTPUT FILE) for a spec of your choice.
4. Explain qualitatively the trends seen in the six graphs of the CHARTS worksheet. Put your explanations in the lab notebook.
5. Use your design tool to design to meet the specs of SPECIFICATIONS section using your measured Q2N2222 parameters and standard resistor values.
6. Verify your design by
   - 6.1. Showing DC I-V plots for highest and lowest value of R_E (that is, for nominal value ±10%); V_CV and I should meet spec
   - 6.2. Showing spiking behavior like Figure 3 for highest and lowest R_E; spiking should occur for an applied 4.5V swing only when DC V_A is set so the collector goes more than 0.5 V below the base.
   - 6.3. Also determine AC ripple currents for 4.5V swing from these plots.
   - 6.4. Tabulate your PSPICE results against the specs.

Measurements

PRECAUTION

Before using the signal generator, ask your TA how to put it in "high-Z" mode to protect the generator from burn-out.

The scope and meters can measure only voltages from a node to ground. You have to be careful in measuring an AC voltage that the instrument does not actually place the node you measure at DC ground, which can upset the bias of the circuit when the DC voltage of the node is not supposed to be at DC ground.

MEASURING OUTPUT RESISTANCE

The output resistance of the mirror is very high, so it is hard to measure. Therefore, in the lab we will artificially assess the role of R_E in the mirror resistance by placing a known resistor value across the output transistor, artificially reducing its output resistance r_O. The setup is shown in Figure 13.

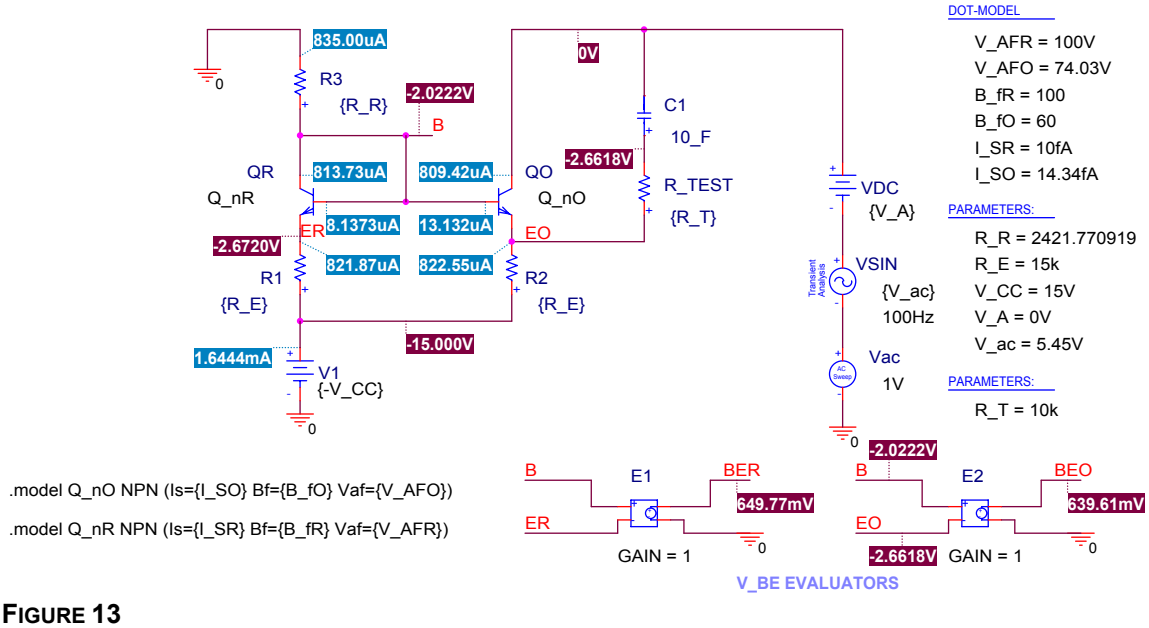

FIGURE 13

Set up to test output resistance formula

The 10F coupling capacitor should be sized smaller, as determined by a PSPICE simulation using a frequency sweep. The capacitor should be just large enough that C does not affect the measurement at the measurement frequency. Plots of mirror resistance vs. value of R_{TEST} should be made for three values of R_E and compared to PSPICE results, such as those in Figure 14 below.

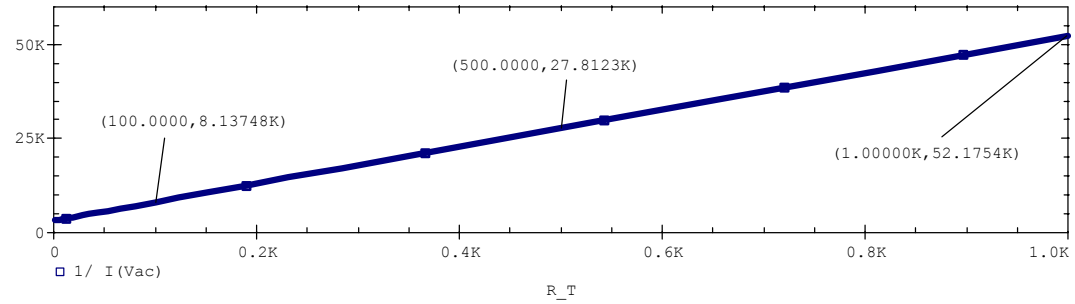

FIGURE 14

PSPICE determination of mirror resistance of circuit in Figure 13 for one value of R_E and V_A= 0 V

The following questions should be answered:

1. What is the formula describing the mirror resistance for Figure 13?
2. Why is a coupling capacitor used in Figure 13?
3. How do your measured results for the mirror resistance compare with your formula – make a table of measured values and values from formula.

TASKS

1. The resistor values should be measured and tabulated in the notebook. Do not accept the color-code values.
2. When the circuit is built, the V_{BE} and V_{CB} values of both transistors should be measured and tabulated with the PSPICE results for comparison. All transistors should be in active mode.
3. Measure the DC I-V curve for your mirror, similar to Figure 4 and mark the coordinates at $V_A = V_B$ and at the compliance voltage.
4. Put the signal generator between the output of the mirror and ground. Apply a sine wave voltage of amplitude V_{ac} and f = 500 Hz. The signal generator allows both an AC voltage and an offset DC voltage to be applied. However, the amount of DC offset is a fraction of the AC amplitude: the larger the AC amplitude, the larger the allowed offset. The goal here is to choose a moderate AC amplitude that is large enough that the offset can be used to take the mirror above and below its compliance voltage, as shown by the spiking behavior illustrated in Figure 3. You can experiment to find a combination of V_{ac} and offset that works.
5. Tabulate your measured results alongside the PSPICE results and the specs.