FIGURE 1

Schematic for folded cascode circuit; capacitances $C_{HF}$ represent the parasitic $C_{p}$ capacitors of transistors Q3 and Q6

FIGURE 2

Gain vs. frequency for $C_{HF} = 0F$, 2pF and 100pF; corner frequency is affected by the load when $C_{HF} = 0F$, but $C_{HF}$ affects the corner as well when $C_{HF} \neq 0$
FIGURE 3
DC transfer curve $V_{\text{OUT}}$ vs. $V_{\text{IN}}$ for amplifier

FIGURE 4
Small-signal gain vs. DC input bias showing fairly constant gain over a window from about $-1.5\text{mV}$ to $+1.5\text{mV}$

FIGURE 5
Large-signal behavior, showing clipping at $V_S = 1.6\text{mV}$, but not at $V_S = 1.4\text{mV}$; upswing and downswing differ, even after subtracting the DC average of the waveform, so some distortion occurs
Merits of this stage
1. Large output swing capability
2. Large gain

Time constant analysis of bandwidth
An open-circuit time constant analysis is presented. A preliminary look at the capacitances by simply pasting the capacitance $C_{HF}$ in various positions (so there is only one capacitor in the circuit besides the load) shows that only the two $C_p$ capacitors shown in Figure 1 matter. Therefore, we focus on these two capacitors, and the load capacitor.

![diagram](image_url)

**Figure 6**
PROBE output file

**Figure 7**
The resistance looking into the CB collector is 1.648 MΩ
FIGURE 8
Resistance seen by the load capacitor is $18.88 \text{k}\Omega \rightarrow f_c = 843 \text{ kHz}$

FIGURE 9
Resistance seen by $C_\mu$ of CB stage is also $18.88 \text{kV} \rightarrow \tau_{C_\mu} = 37.8 \text{ ns} \rightarrow$ corner with both $C_L$ and $C_\mu = 703 \text{ kHz}$; CB circuit above dashed line is replaced by its input resistance $R_{\text{IN,CB}}$

FIGURE 10
Resistance seen by $C_\mu$ of mirror output transistor Q6 is $37.39 \text{k}\Omega$, basically $\rightarrow \tau = 74.8 \text{ ns}$; corner with all three caps is 528 kHz
Summary
Because of the large resistors in this circuit, the bandwidth is not very large. However, there is no limitation due to the Miller effect.