LECTURE 020 – ECE 4430 REVIEW II
(READING: GHLM - Chap. 2)

Objective

The objective of this presentation is:

1.) Identify the prerequisite material as taught in ECE 4430

2.) Insure that the students of ECE 6412 are adequately prepared

Outline

- Models for Integrated-Circuit Active Devices
- Bipolar, MOS, and BiCMOS IC Technology
- Single-Transistor and Multiple-Transistor Amplifiers
- Transistor Current Sources and Active Loads

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BIPOLAR, MOS, AND BICMOS IC TECHNOLOGY

Bipolar Technology

- *npn* BJT technology
- Compatible *pnp* BJTs
- Modifications to the standard *npn* BJT technology

Major Processing Steps for a Junction Isolated BJT Technology

Start with a *p* substrate.

1. Implantation of the buried n^+ layer
2. Growth of the epitaxial layer
3. p^+ isolation diffusion
4. Base *p*-type diffusion
5. Emitter n^+ diffusion
6. p^+ ohmic contact
7. Contact etching
8. Metal deposition and etching
9. Passivation and bond pad opening

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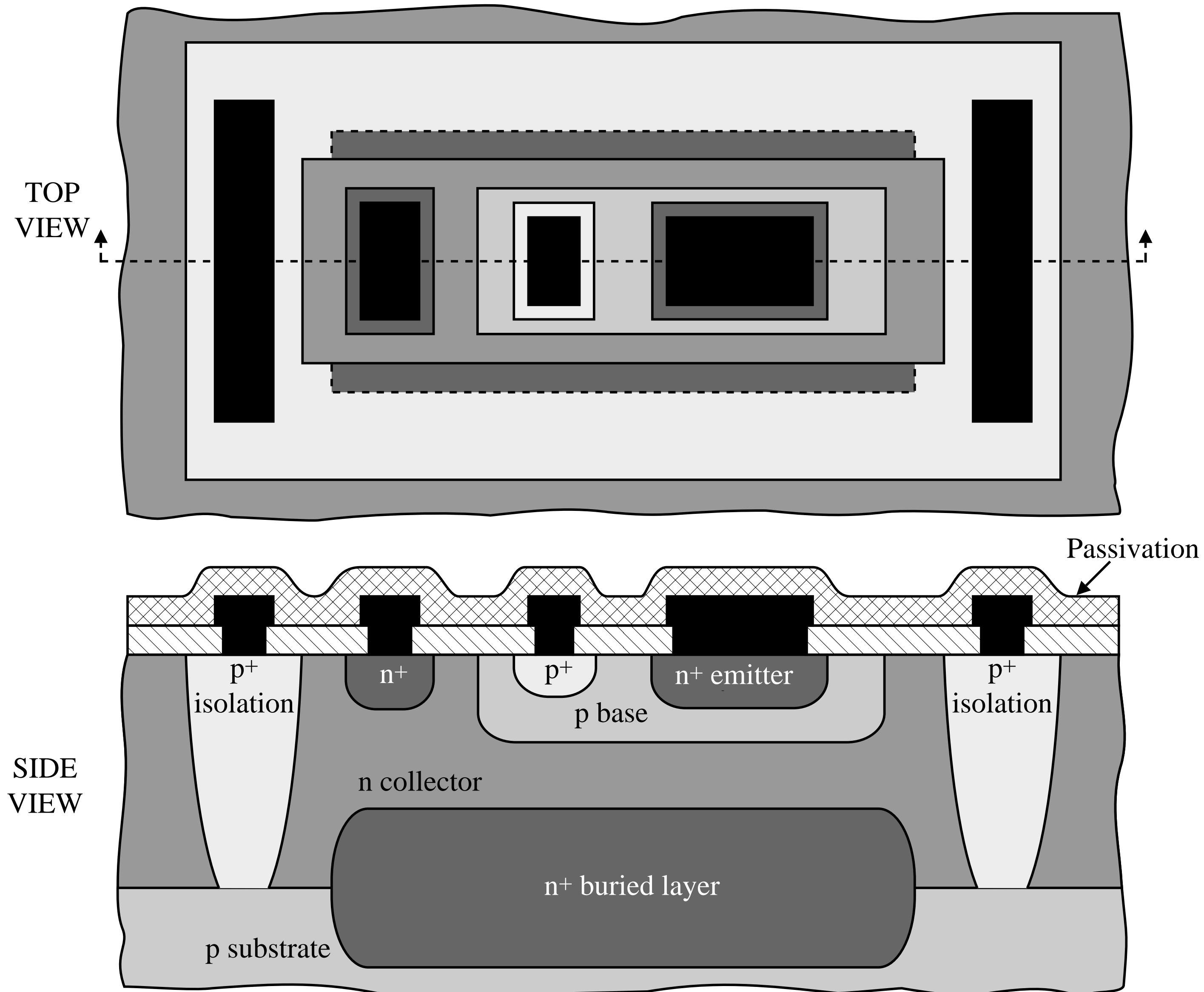
Integrated Circuit NPN BJT



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Substrate *pnp* BJT

Collector is connected to the substrate potential which is the most negative DC potential.

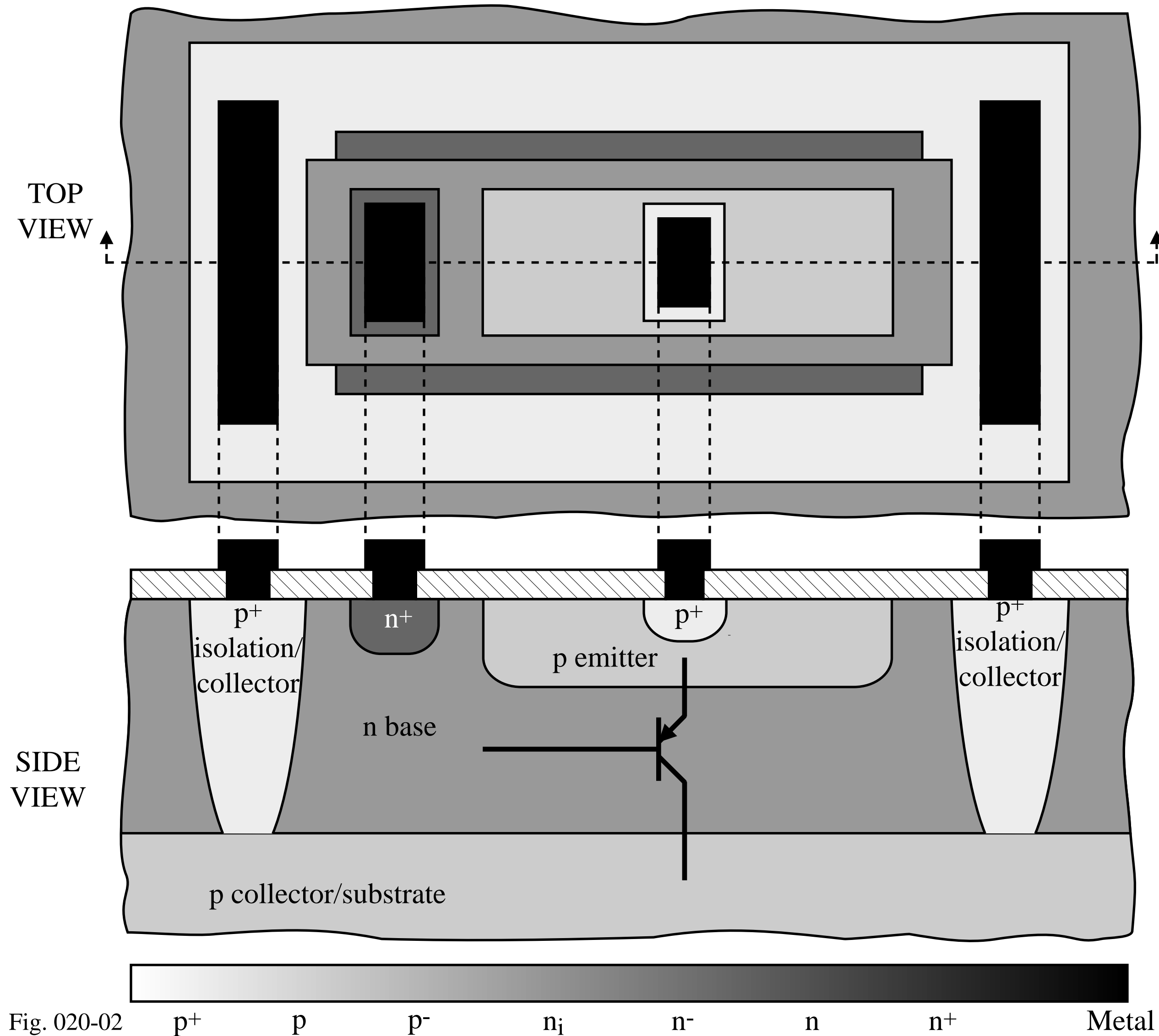

Fig. 020-02

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Lateral *pnp* BJT

Collector is not constrained to a fixed dc potential.

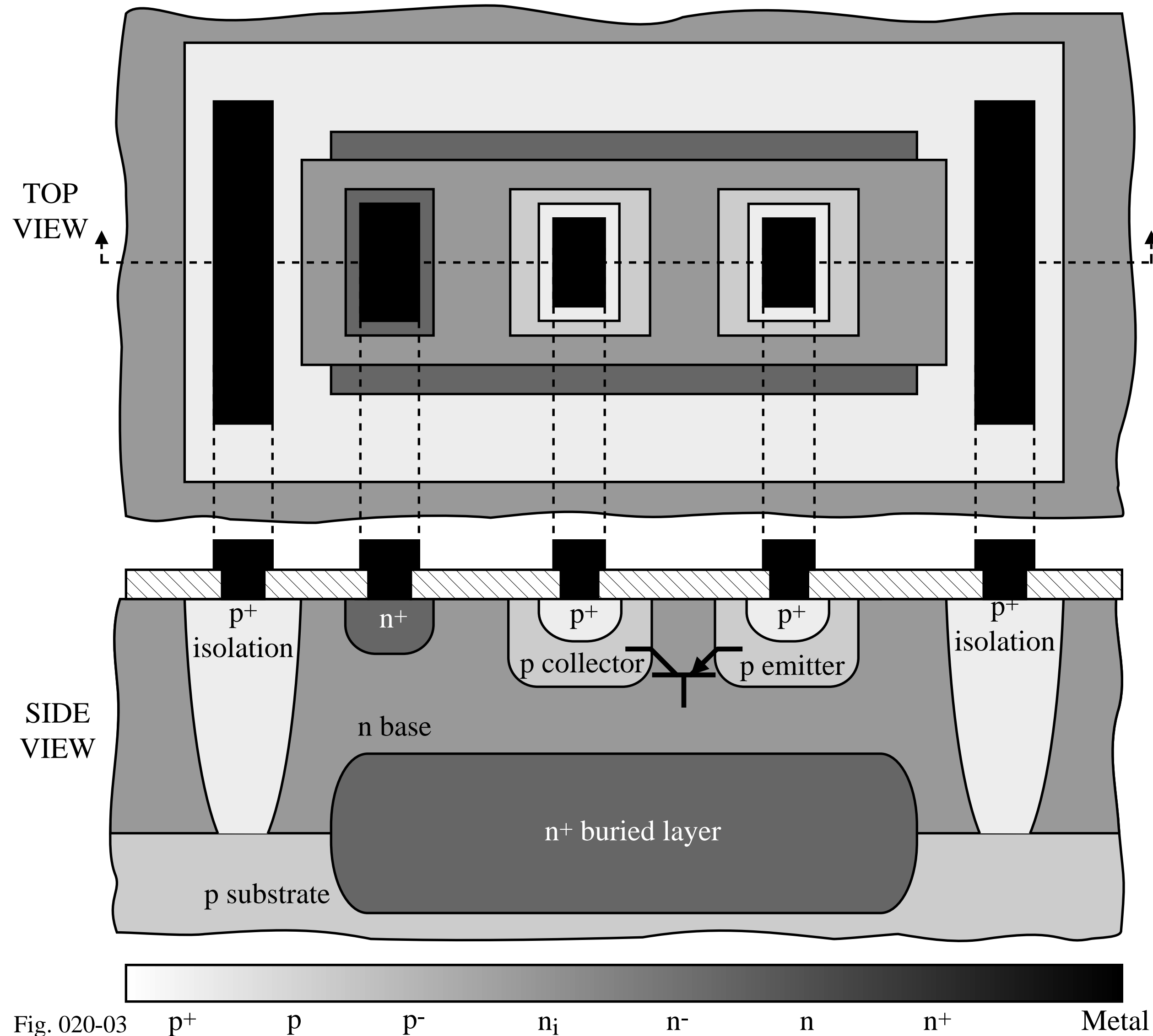

Fig. 020-03

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CMOS Technology

N-Well CMOS Fabrication Major Steps:

1.) Implant and diffuse the n-well
2.) Deposition of silicon nitride
3.) n-type field (channel stop) implant
4.) p-type field (channel stop) implant
5.) Grow a thick field oxide (FOX)
6.) Grow a thin oxide and deposit polysilicon
7.) Remove poly and form LDD spacers
8.) Implantation of NMOS S/D and n-material contacts
9.) Remove spacers and implant NMOS LDDs
10.) Repeat steps 8.) and 9.) for PMOS
11.) Anneal to activate the implanted ions
12.) Deposit a thick oxide layer (BPSG - borophosphosilicate glass)
13.) Open contacts, deposit first level metal and etch unwanted metal
14.) Deposit another interlayer dielectric (CVD SiO_2), open vias and deposit second level metal
15.) Etch unwanted metal, deposit a passivation layer and open over bonding pads

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Typical CMOS Technology

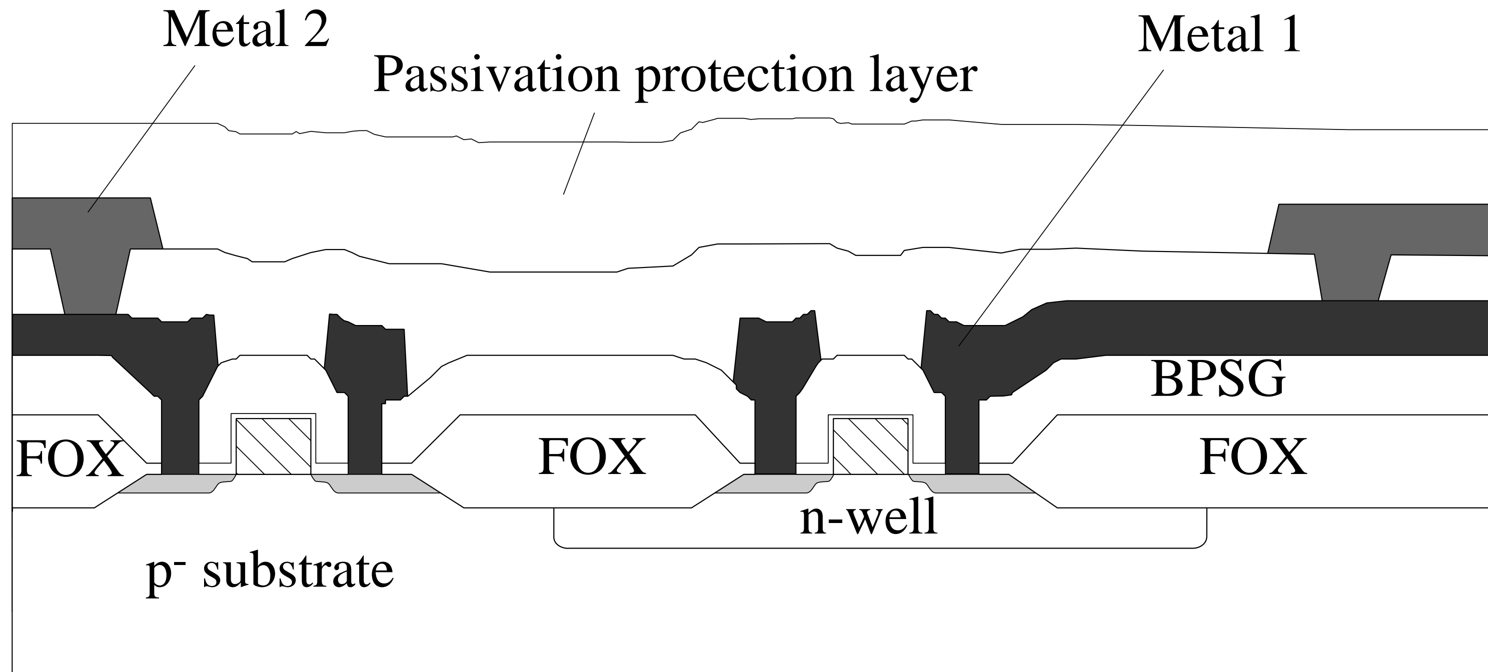
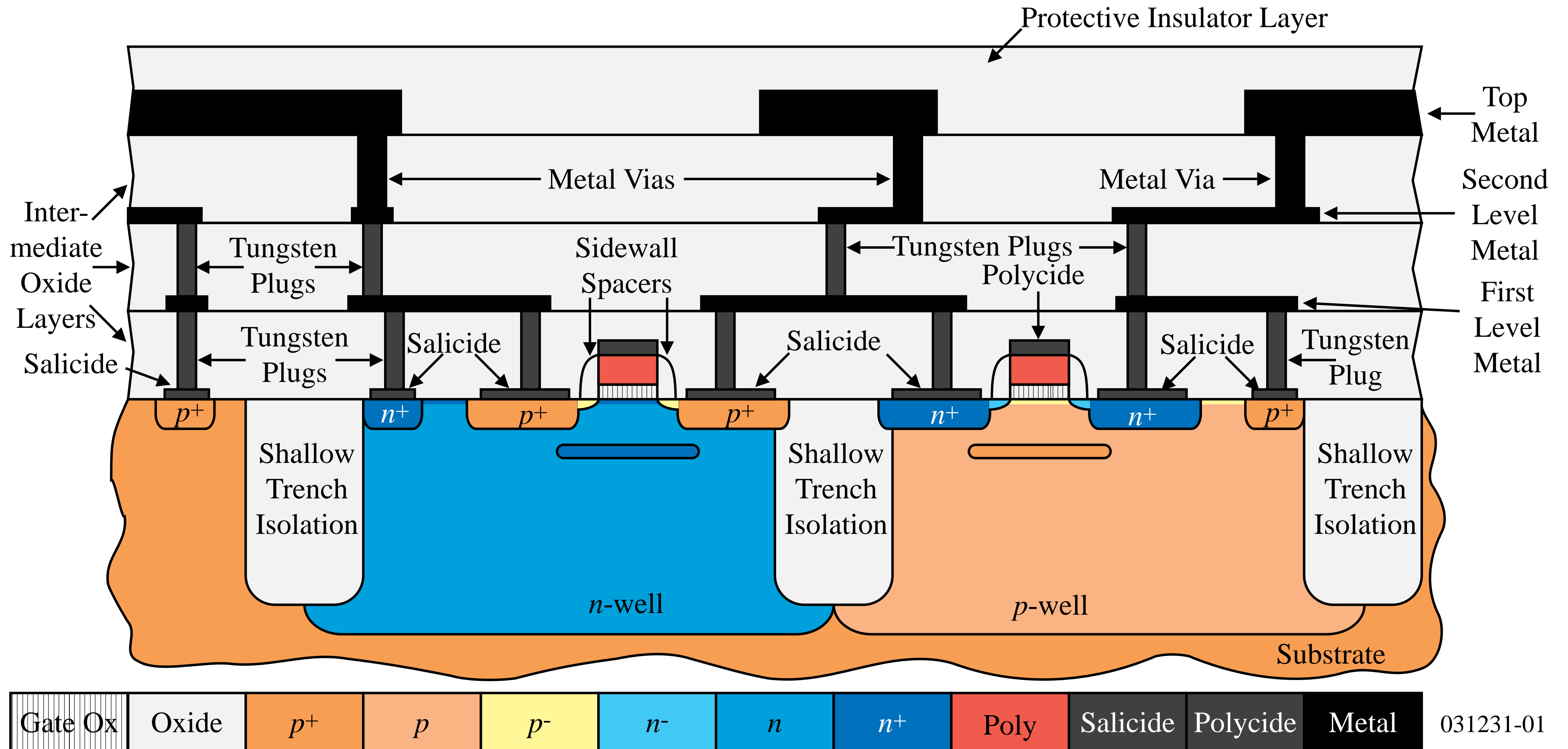


Fig. 020-04

p-well process is similar but starts with a p-well implant rather than an n-well implant.

Modern CMOS Technology (DSM)

Uses shallow trench isolation to electrically and physically isolate transistors. Typical of today's deep submicron technology.



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Example of 0.5μm CMOS Technology

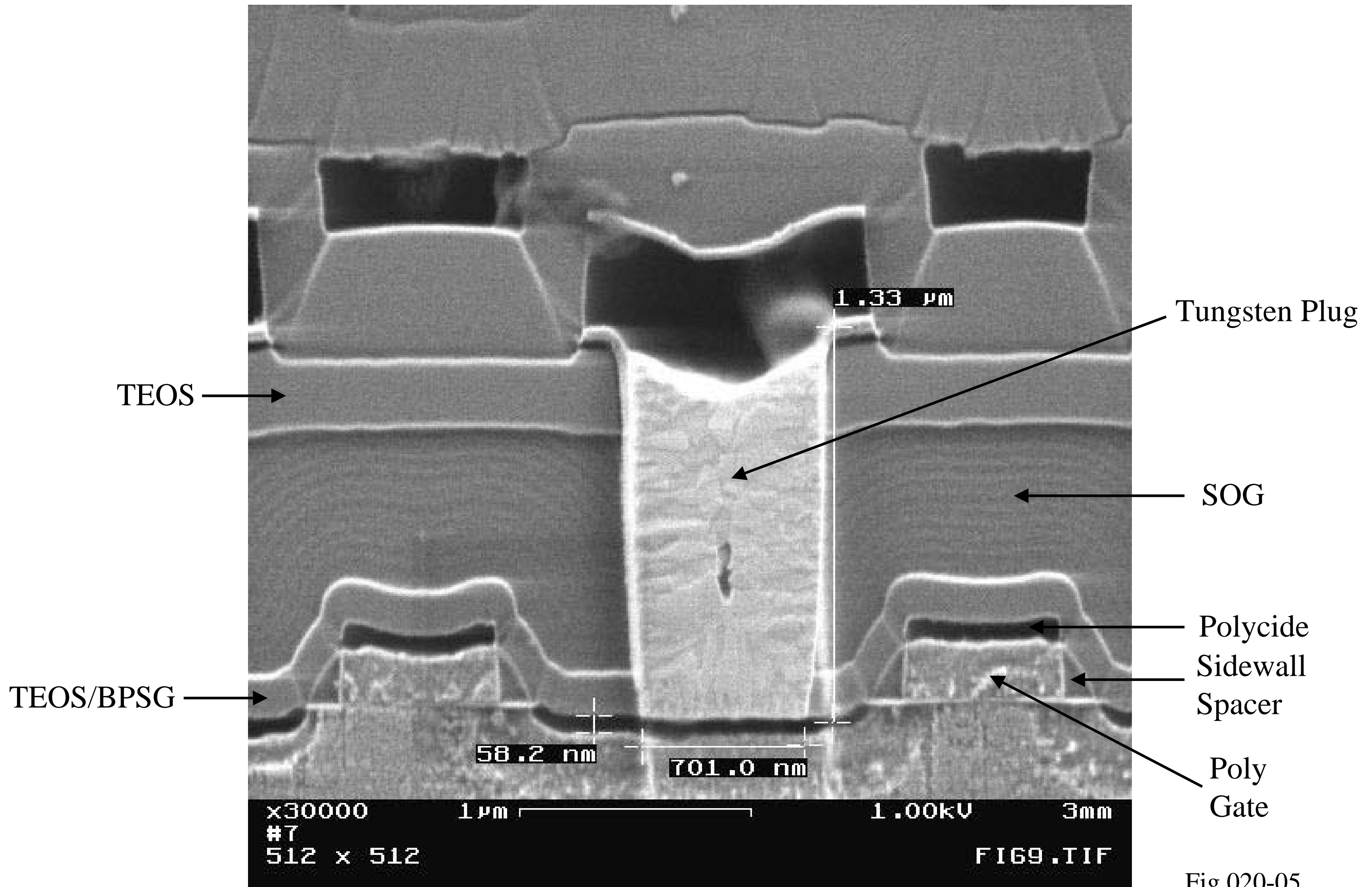

Fig.020-05

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BiCMOS Technology

The following steps are typical of a 0.5μm BiCMOS process typical of today's deep submicron technologies.

Masking Sequence:

1. Buried n^+ layer
2. Buried p^+ layer
3. Collector tub
4. Active area
5. Collector sinker
6. n-well
7. p-well
8. Emitter window
9. Base oxide/implant
10. Emitter implant
11. Poly 1
12. NMOS lightly doped drain
13. PMOS lightly doped drain
14. n^+ source/drain
15. p^+ source/drain
16. Silicide protection
17. Contacts
18. Metal 1
19. Via 1
20. Metal 2
21. Via 2
22. Metal 3
23. Nitride passivation

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BiCMOS Technology Illustration

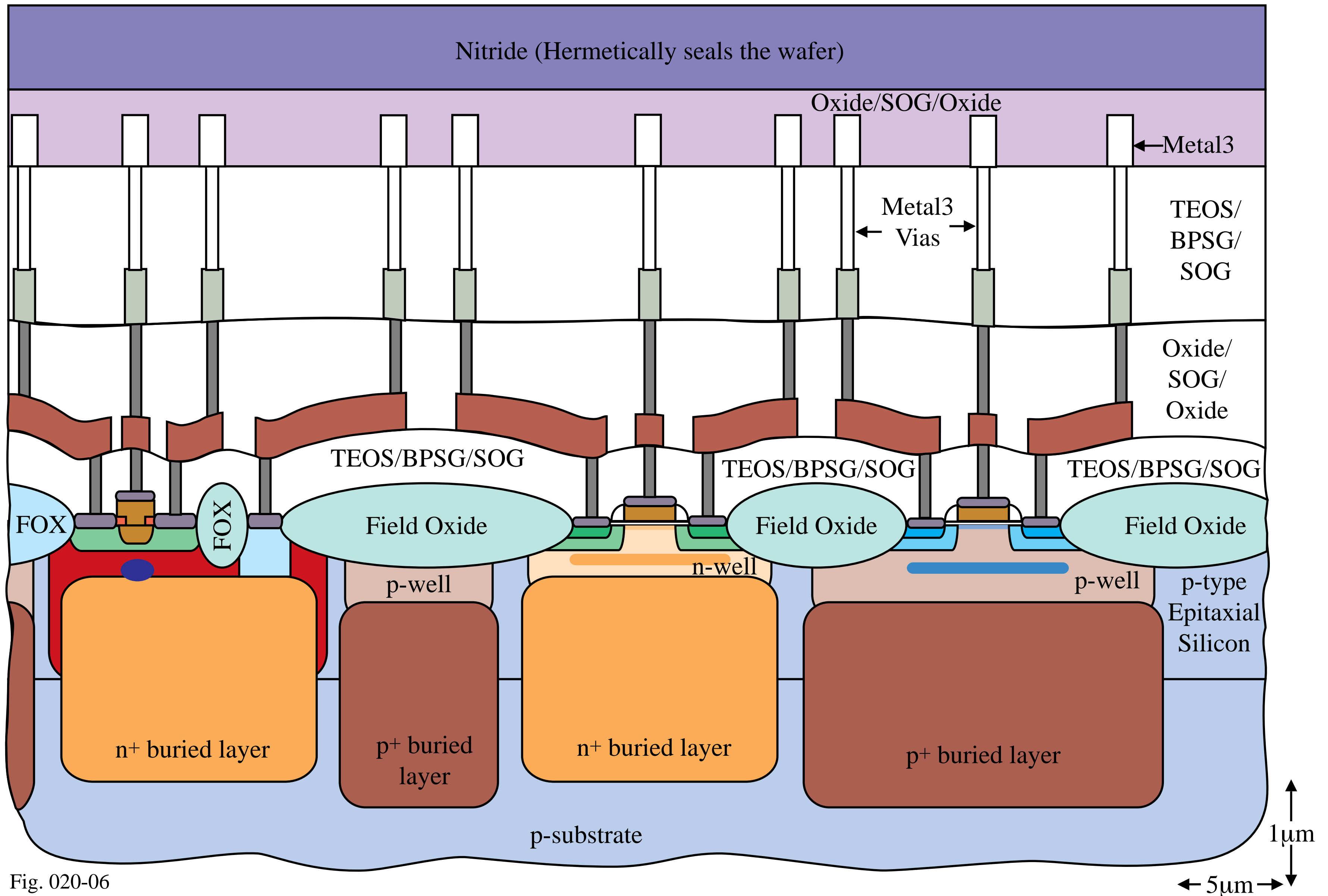

Fig. 020-06

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Passive Components - Collector-Base Capacitance (C_μ)

Illustration:

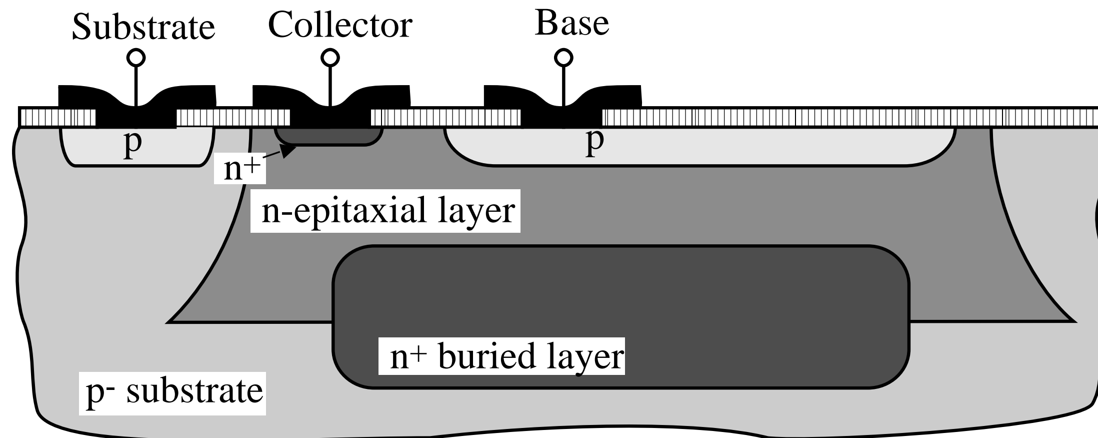

Fig. 020-07

Model:

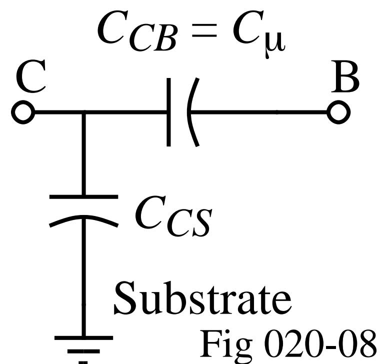

Fig 020-08

Sidewall contribution:

$$A_{sidewall} = P \cdot d\,\frac{\pi}{2}$$

where

P = perimeter of the capacitor

d = depth of the diffusion

Values (Includes the bottom plus sidewall capacitance):

$C_\mu \approx 1\text{fF}/\mu\text{m}^2$ (dependent on the reverse bias voltage)

Can also have base-emitter capacitance and collector-substrate capacitance

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MOS Capacitors

Polysilicon-Oxide-Channel for Enhancement MOSFETs

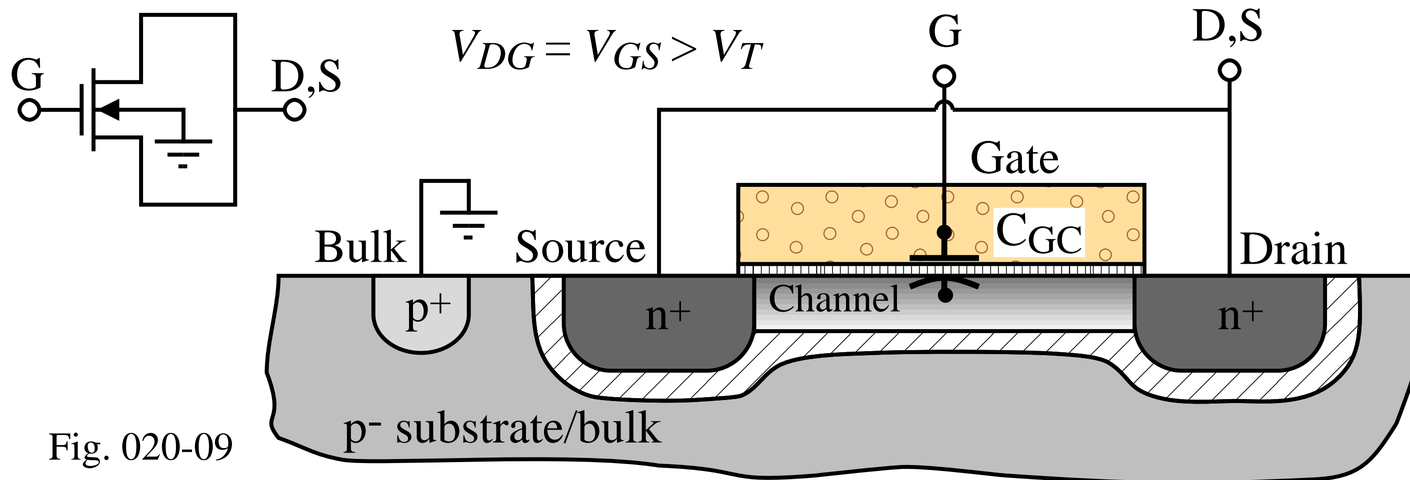

Fig. 020-09

Comments:

- The capacitance variation is achieved by changing the mode of operation from depletion (minimum capacitance) to inversion (maximum capacitance).
- Capacitance = $C_{GS} \approx C_{ox}W \cdot L$
- Channel must be formed, therefore $V_{GS} > V_T$
- With $V_{GS} > V_T$ and $V_{DS} = 0$, the transistor is in the active region.
- LDD transistors will give lower Q because of the increase of series resistance.

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MOS Capacitors

Bulk tuning of the polysilicon-oxide-channel capacitor (0.35µm CMOS)

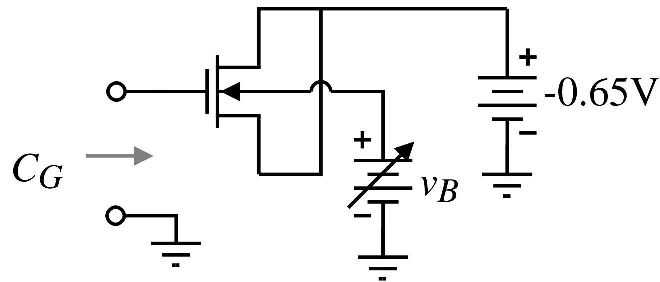
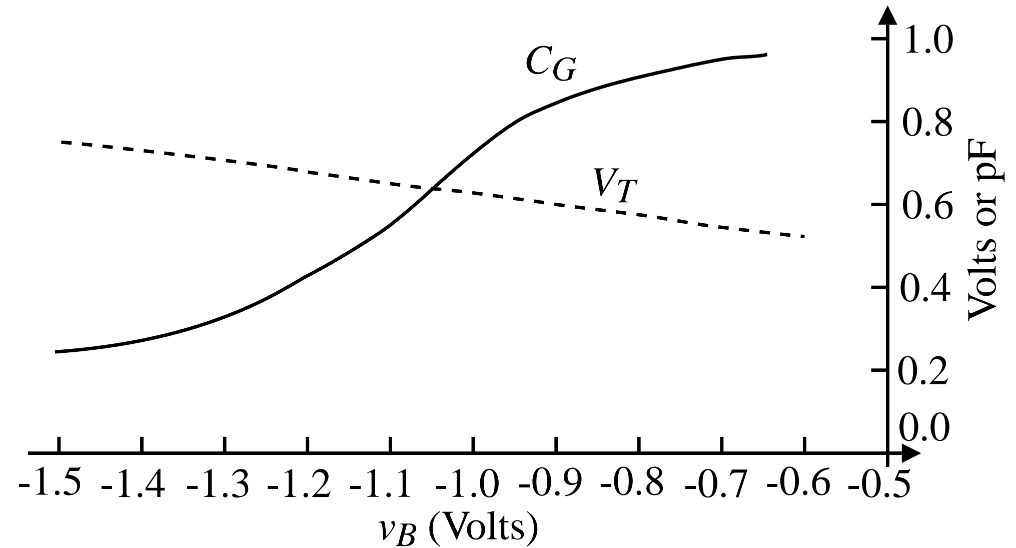


Fig. 020-10



$C_{max}/C_{min} \approx 4$

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Accumulation-Mode Capacitor[1,2]

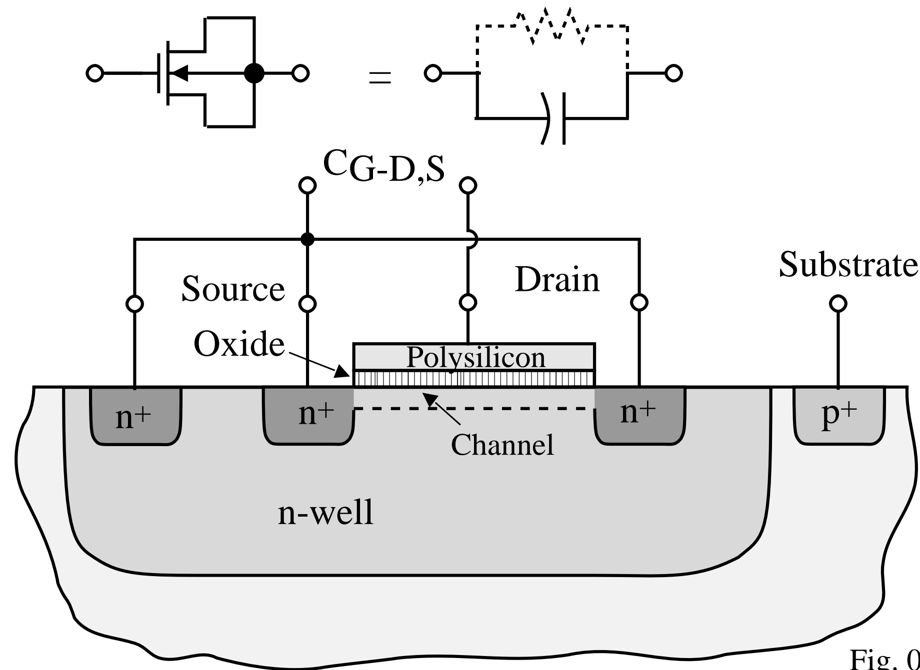

Fig. 020-11

Comments:

- Again, the capacitor variation is achieved by moving from the depletion (min. C) to accumulation (max. C)
- ±30% tuning range (Tuned by the voltage across the capacitor terminals)
- $Q \approx 25$ for 3.1pF at 1.8 GHz (optimization leads to Qs of 200 or greater)

[1] T. Soorapanth, et. al., "Analysis and Optimization of Accumulation-Mode Varactor for RF ICs," Proc. 1998 Symposium on VLSI Circuits, *Digest of Papers*, pp. 32-33, 1998.

[2] R. Castello, et. al., "A ±30% Tuning Range Varactor Compatible with future Scaled Technologies," Proc. 1998 Symposium on VLSI Circuits, *Digest of Papers*, pp. 34-35, 1998.

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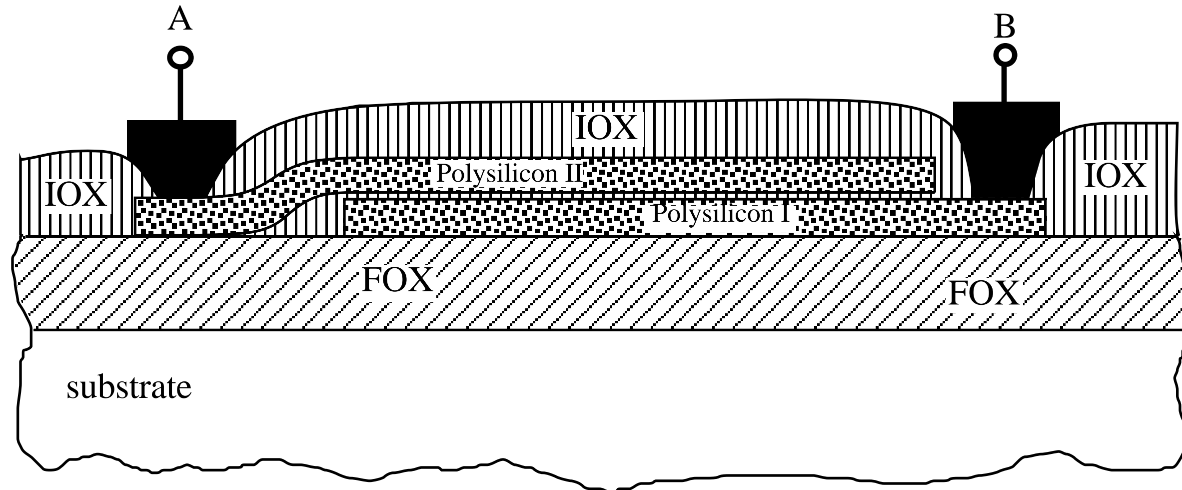
Polysilicon-Oxide-Polysilicon (Poly-Poly)



Best possible capacitor for analog circuits

Less parasitics

Voltage independent

Capacitor Errors:

1.) Oxide gradients

2.) Edge effects

3.) Parasitics

4.) Voltage dependence

5.) Temperature dependence

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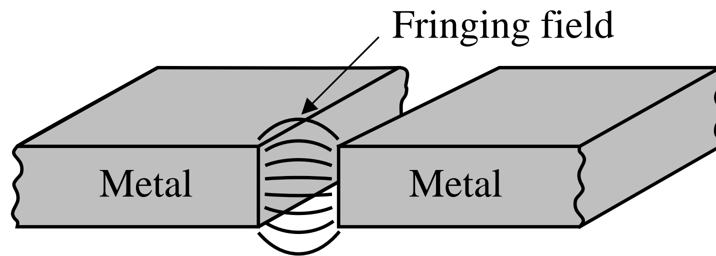
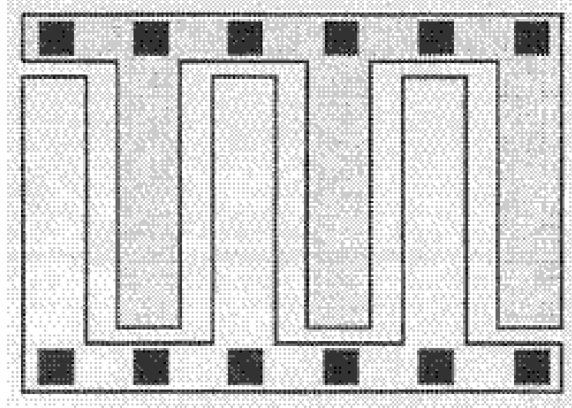
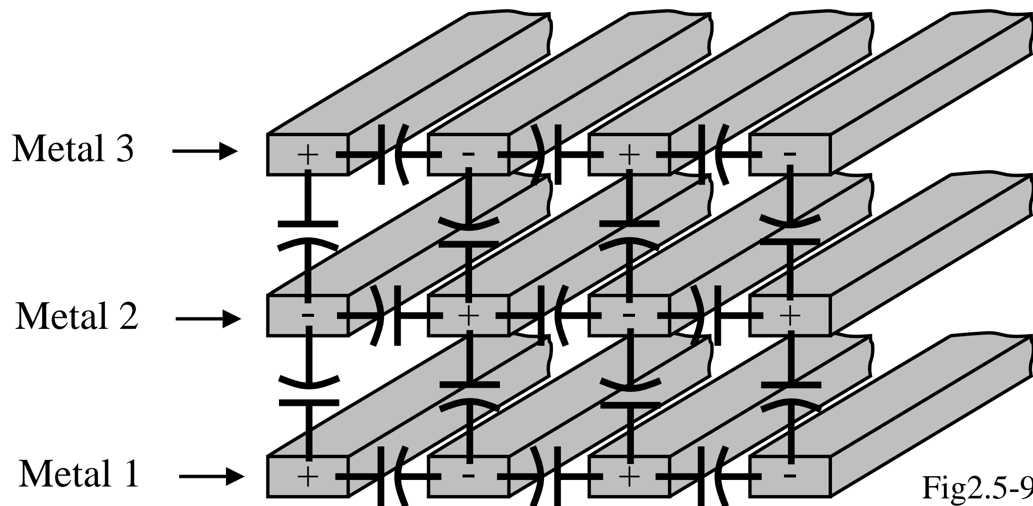
Horizontal Metal Capacitors

Capacitance between conductors on the same level and use lateral flux.

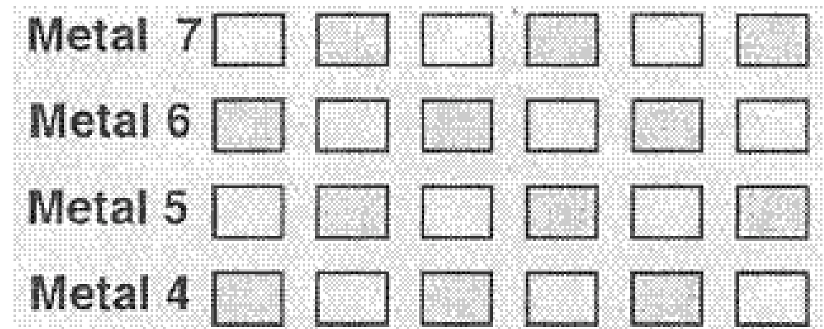


Top view:





Side view:



These capacitors are sometimes called fractal capacitors because the fractal patterns are structures that enclose a finite area with an infinite perimeter.

The capacitor/area can be increased by a factor of 10 over vertical flux capacitors.

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Integrated Circuit Resistors - Layout

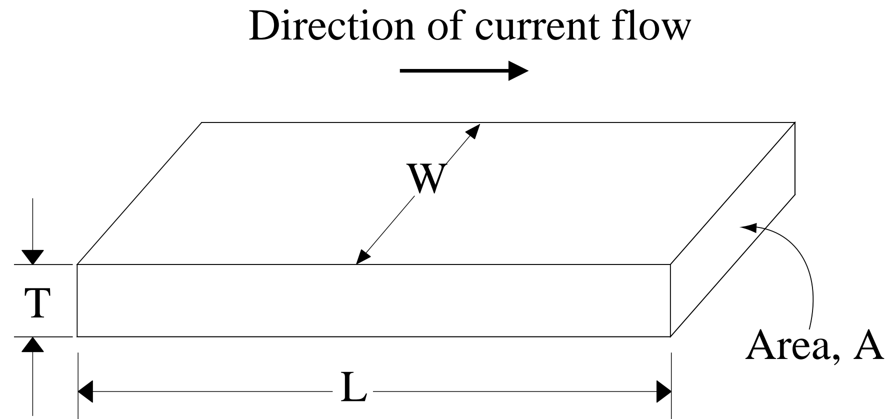

Fig. 020-14/170-02

Resistance of a conductive sheet is expressed in terms of

$$R = \frac{\rho L}{A} = \frac{\rho L}{WT} \ (\Omega)$$

where

ρ = resistivity in Ω-m

Ohms/square:

$$R = \left(\frac{\rho}{T}\right)\frac{L}{W} = \rho_S \frac{L}{W} \ (\Omega)$$

where

ρ_S is a sheet resistivity and has the units of ohms/square

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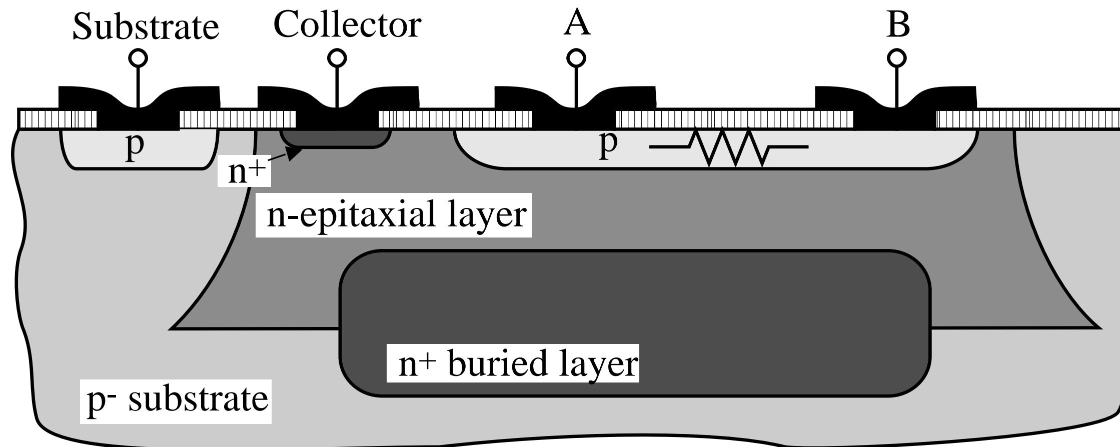
Base and Emitter Diffused Resistors

Cross-section of a Base Resistor:



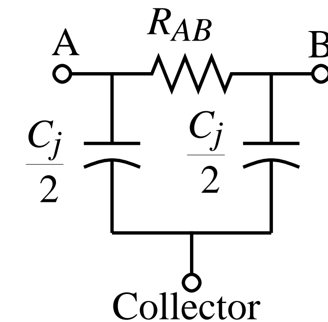


Fig. 020-15/170-03

Comments:

Sheet resistance ≈ 100 Ω/sq. to 200 Ω/sq.

TCR = +1500ppm/°C

Note:

$$\frac{1\%}{°C} = \frac{10^4 ppm}{°C}$$

Emitter Resistor:

Sheet resistance ≈ 2 Ω/sq. to 10 Ω/sq. (Generally too small to make sufficient resistance in reasonable area)

TCR = +600ppm/°C

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Epitaxial Pinched Resistor

Good for large values of sheet resistance.

Cross-section:

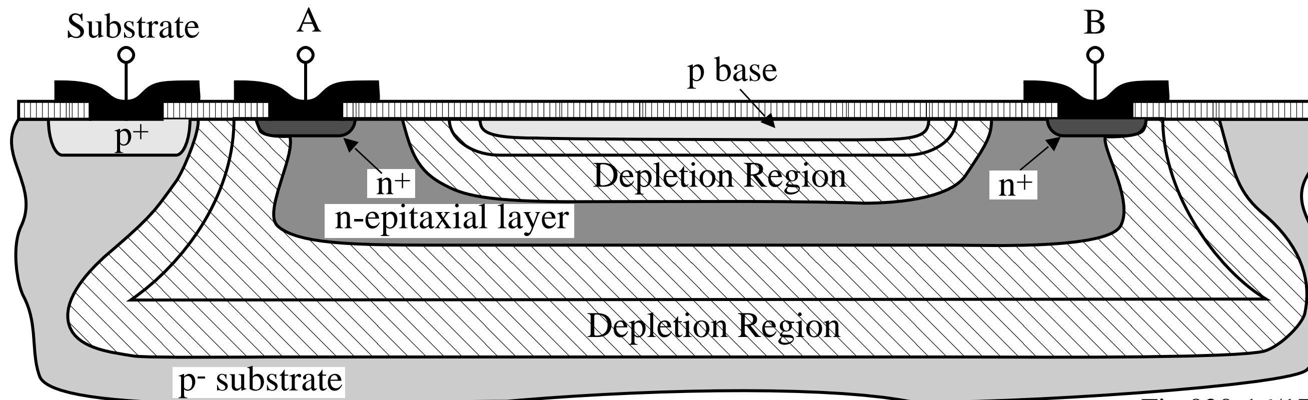
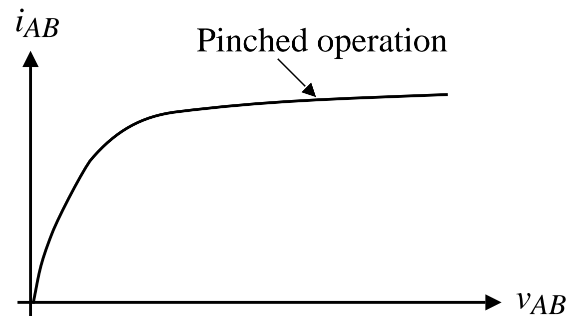


Fig 020-16/170-05

IV Curves and Model:



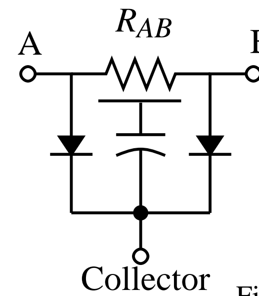


Fig. 020-17/170-06

Comments:

Sheet resistance is 4 to 10kΩ/sq.

Voltage across the resistor is limited to 6V or less because of breakdown

TCR ≈ 2500ppm/°C

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MOS Resistors - Source/Drain Resistor

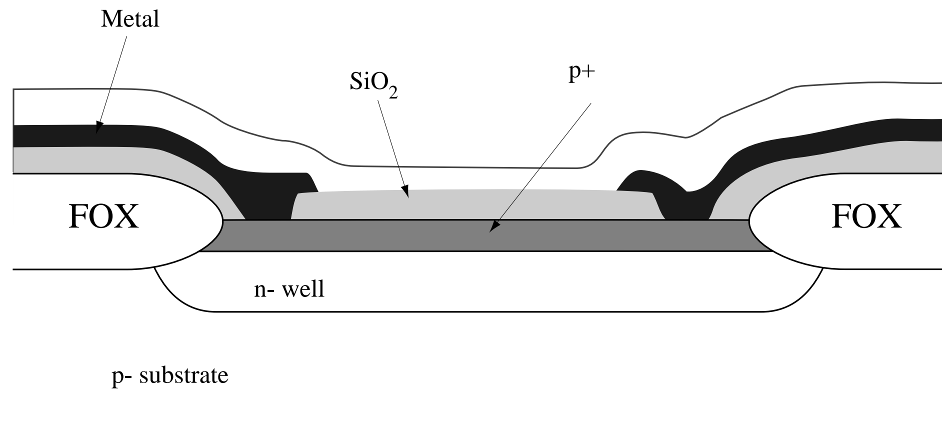

Fig. 020-18

Diffusion:

10-100 ohms/square

Absolute accuracy = ±35%

Relative accuracy = 2% (5 μm), 0.2% (50 μm)

Temperature coefficient = 1500 ppm/°C

Voltage coefficient ≈ 200 ppm/V

Ion Implanted:

500-2000 ohms/square

Absolute accuracy = ±15%

Relative accuracy = 2% (5 μm), 0.15% (50 μm)

Temperature coefficient = 400 ppm/°C

Voltage coefficient ≈ 800 ppm/V

Comments:

- Parasitic capacitance to well is voltage dependent.
- Piezoresistance effects occur due to chip strain from mounting.

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Polysilicon Resistor

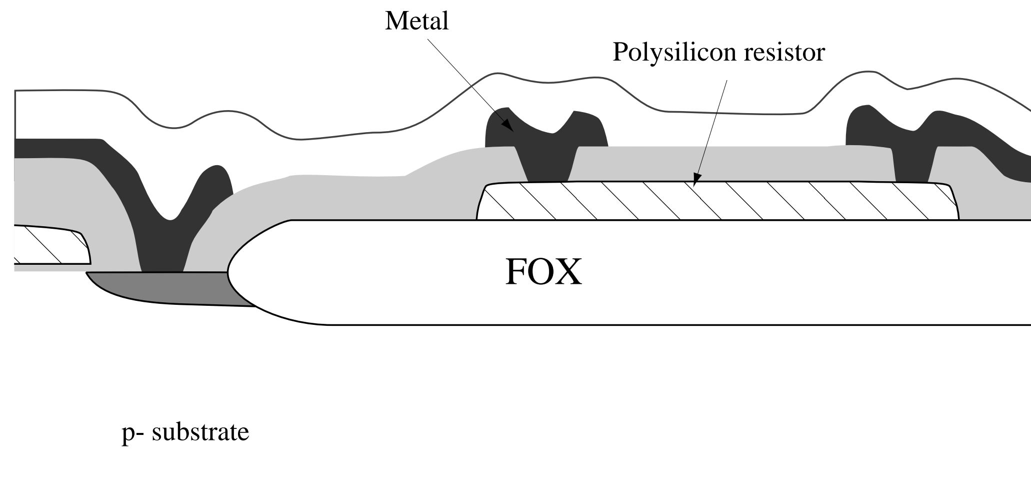

Fig. 020-19

30-100 ohms/square (unshielded)

100-500 ohms/square (shielded)

Absolute accuracy = ±30%

Relative accuracy = 2% (5 μm)

Temperature coefficient = 500-1000 ppm/°C

Voltage coefficient ≈ 100 ppm/V

Comments:

- Used for fuzes and laser trimming
- Good general resistor with low parasitics

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N-well Resistor

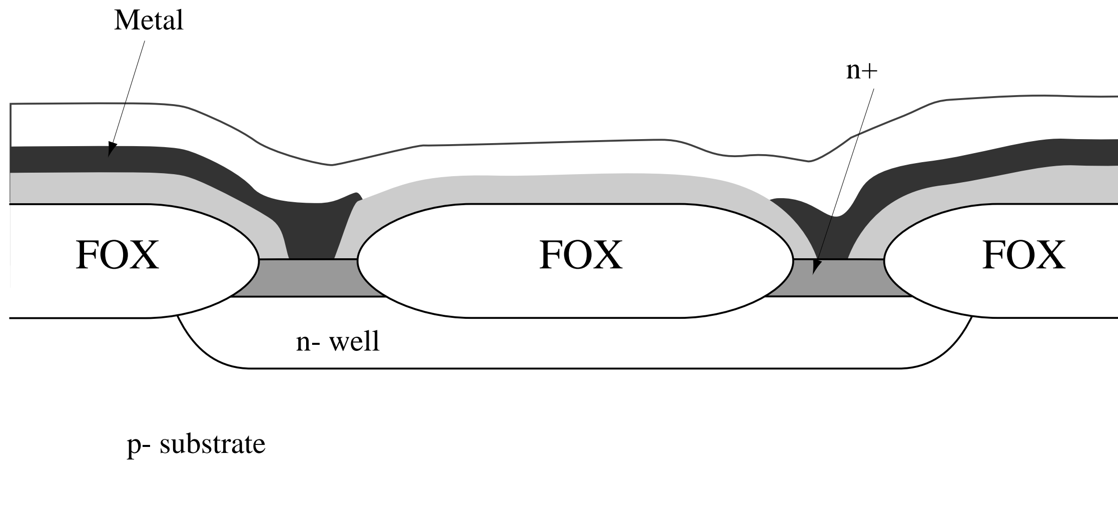

Fig. 020-20

1000-5000 ohms/square

Absolute accuracy = ±40%

Relative accuracy ≈ 5%

Temperature coefficient = 4000 ppm/°C

Voltage coefficient is large ≈ 8000 ppm/V

Comments:

- Good when large values of resistance are needed.
- Parasitics are large and resistance is voltage dependent

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Integrated Circuit Passive Component Performance Summary

Component Type	Range of Values	Absolute Accuracy	Relative Accuracy	Temperature Coefficient	Voltage Coefficient
MOS Capacitor	0.35-1.0 fF/μm²	10%	0.1%	20ppm/°C	±20ppm/V
Poly-Poly Capacitor	0.3-1.0 fF/μm²	20%	0.1%	25ppm/°C	±50ppm/V
Base Diffused	100-200Ω/sq.	±20%	0.2%	+1750ppm/°C	-
Emitter Diffused	2-10Ω/sq.	±20%	±2%	+600ppm/°C	-
Base Pinched	2k-10kΩ/sq.	±50%	±10%	+2500ppm/°C	Poor
Epitaxial Pinched	2k-5kΩ/sq.	±50%	±7%	+3000ppm/°C	Poor
S/D Diffused	10-100 Ω/sq.	35%	2%	1500ppm/°C	200ppm/V
Implanted Resistor	0.5-2 kΩ/sq.	15%	2%	400ppm/°C	800ppm/V
Poly Resistor	30-200 Ω/sq.	30%	2%	1500ppm/°C	100ppm/V
n-well Resistor	1-10 kΩ/sq.	40%	5%	8000ppm/°C	10kppm/V
Thin Film	0.1k-2kΩ/sq.	±5-±20%	±0.2-±2%	±10 to ±200ppm/°C	-

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SUMMARY

- Bipolar Technology
  - Vertical NPN transistor
  - Substrate PNP transistor
  - Lateral PNP transistor
- CMOS Technology
  - Substrate BJT
  - Lateral BJT
- BiCMOS Technology
  - Vertical NPN transistor
  - CMOS transistors
- Passive Components Compatible with IC Technology
  - Resistors
  - Capacitors

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