ECE 304 Exam 3 Spring 05 Solutions

NOTE: IN ALL CASES

1. Solve the problem on scratch paper
2. Once you understand your solution, put your answer on the answer sheet
3. Follow your answer with an outline of your solution. No points for answer without an outline of the solution. A mish-mash of computation is not an acceptable outline.

PRINT your name at the top of each answer sheet

Assume V_{TH} = 25.864 mV in all problems and maximum collector-base forward bias in saturation is V_{CB} = 0 V. Where V_{BE} is needed, evaluate it using $V_{BE} = V_{TH}\,\ell n(I_C/I_S)$.

Problem 1: Voltage follower

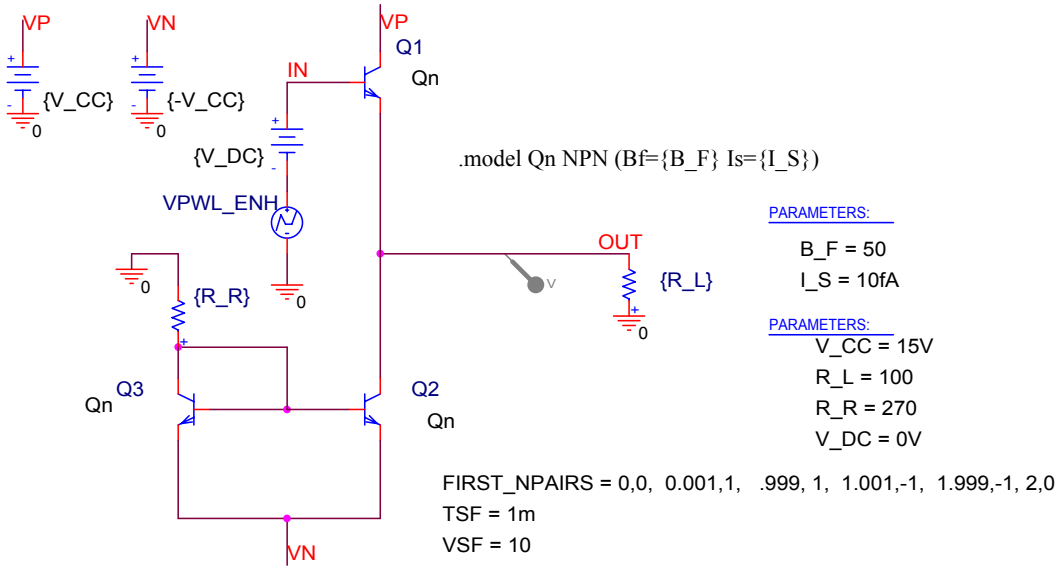

FIGURE 1

Voltage follower for Problem 1

A square-wave voltage is input as signal, as shown in Figure 2.

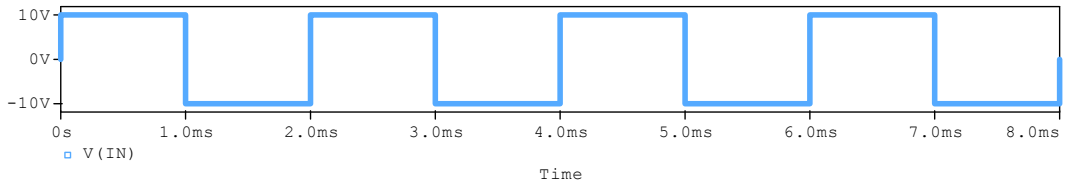

FIGURE 2

Input square wave $\upsilon_{IN}(t) = 10\ sq(t)$

FUNCTION *sq*(t) IS A UNIT AMPLITUDE SQUARE WAVE, +1 IN POSITIVE HALF-CYCLE AND –1 IN NEGATIVE HALF CYCLE. The input voltage is $\upsilon_{IN}(t) = 10\ sq(t)$.

1. Construct the DC input-output transfer curve υ_{OUT} vs. υ_{IN}. Label all corners and levels.

ANSWER:

See Figure 3 next page.

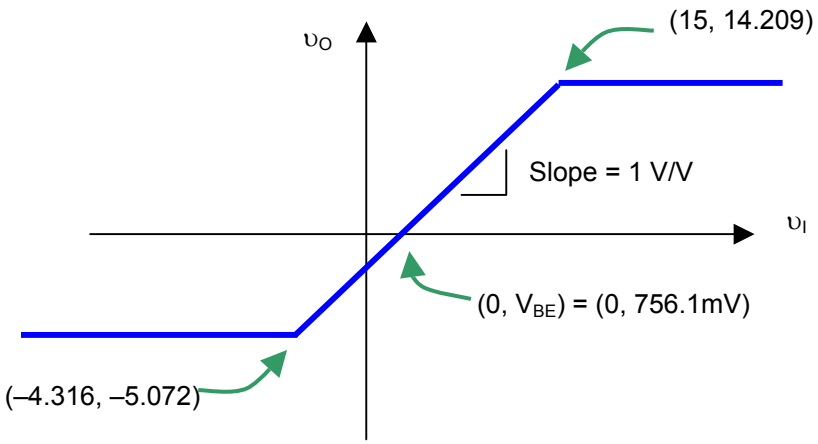

FIGURE 3
Input-output transfer curve for voltage follower

OUTLINE:

As this is a voltage follower, the gain should be close to 1 V/V, with the output following the input, but V_{BE} lower.

MIRROR

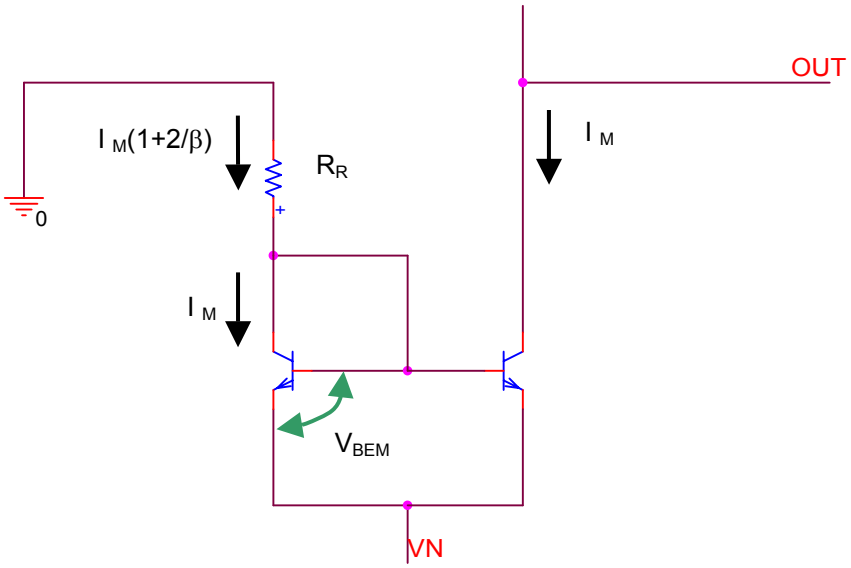

FIGURE 4
Mirror schematic

The mirror current is given by Ohm's law as

EQ. 1

$$I_M = \frac{V_{CC} - V_{BEM}}{R_R(1+2/\beta)}.$$

The diode law then determines V_{BEM} by iteration:

EQ. 2

$$V_{BEM} = V_{TH}\ell n\left(\frac{I_M}{I_S}\right) = V_{TH}\ell n\left(\frac{V_{CC} - V_{BEM}}{I_S R_R(1+2/\beta)}\right) = 756.6 \text{ mV},$$

$$I_M = 50.72 \text{ mA}.$$

ZERO OUTPUT CASE

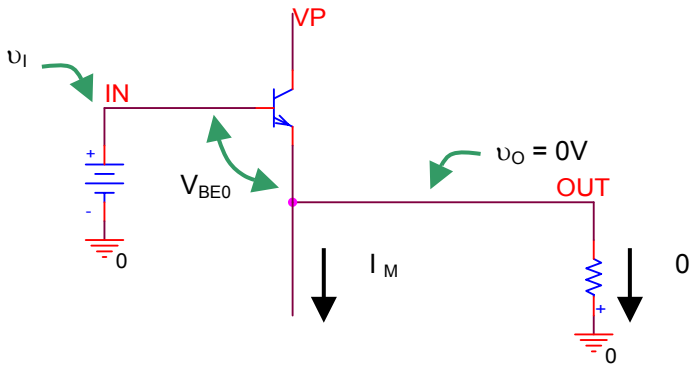

FIGURE 5
Zero output case

For $\upsilon_O = 0V$, $\upsilon_I = V_{BE0} = V_{TH}\ell n\left(\frac{I_M}{I_S(1+1/\beta)}\right) = 756.1$ mV

MAXIMUM OUTPUT CASE

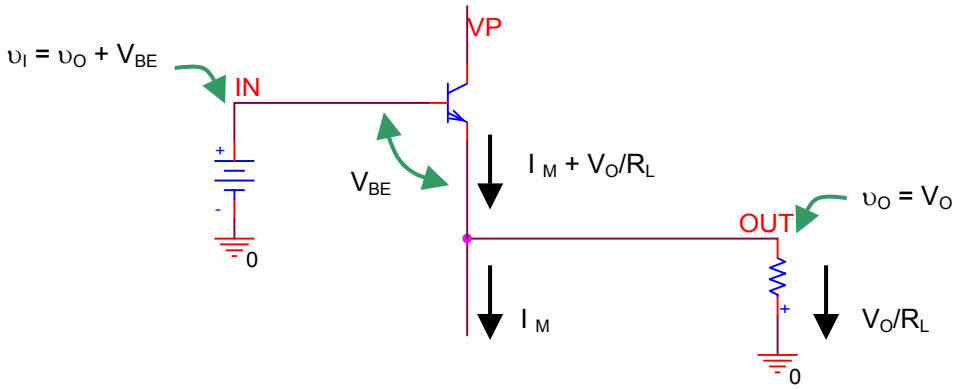

FIGURE 6
Maximum output voltage case; transistor is saturated

At the maximum input voltage, the base can exceed the collector by zero voltage ($V_{CB}(Sat) = 0V$ is given). Therefore, the transistor saturates when $\upsilon_I = V_{CC}$. At this input voltage, the output voltage is V_{BE} lower, where V_{BE} is given by the diode law as

EQ. 3

$$V_{BE} = V_{TH}\ell n\left(\frac{I_M + V_O/R_L}{I_S(1+1/\beta)}\right) = V_{TH}\ell n\left(\frac{I_M + (V_{CC} - V_{BE})/R_L}{I_S(1+1/\beta)}\right) = 790.7 \text{ mV}.$$

EQ. 3 is solved by iteration. Then $\upsilon_O = \upsilon_I - V_{BE} = 15 - 790.7$ mV $= 14.209$ V.

LOW VOLTAGE OUTPUT

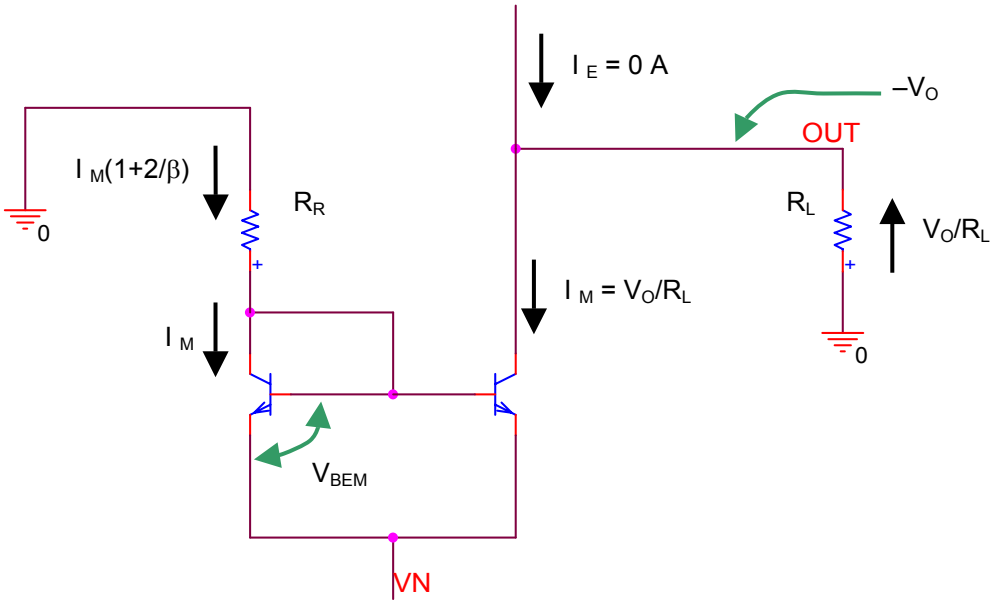

FIGURE 7

In the low voltage case $\upsilon_O = -V_O$ and the transistor is limited by cutoff

Because all Early voltages are infinite, the mirror current remains I_M. Invoking cutoff as the limiting mechanism, KCL at the emitter node of the input transistor provides

EQ. 4

$$I_M = V_O/R_L \rightarrow V_O = I_M R_L = 5.072\ \text{V},$$

and $\upsilon_O = -V_O = -5.072$ V. If the transistor is actually in cutoff, $V_{BE} = 0$ V, which means that $\upsilon_I = \upsilon_O$. However, the transistor turn-on is exponential (that is, very rapid). As the output voltage increases above the cutoff value of 5.072 V, V_{BE} will rapidly increase, and the slope of υ_O vs. υ_I will quickly approach 1 V/V again. Therefore, to estimate the υ_I in the low voltage case, we extend the unity slope line for positive output voltages already found down to negative output voltages. The input voltage is then approximately given by $\upsilon_I \approx \upsilon_O + V_{BE}(\upsilon_O = 0\text{V}) = -5.072 + 756.6\ \text{mV} = -4.316\text{V}$.

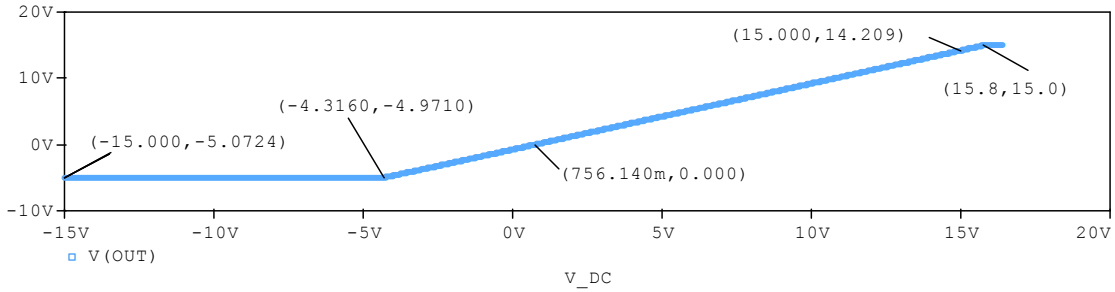

FIGURE 8

PSPICE υ_O vs. υ_I transfer curve; the value of $\upsilon_{IN} = -4.316$V locates the end of the unity slope region pretty accurately

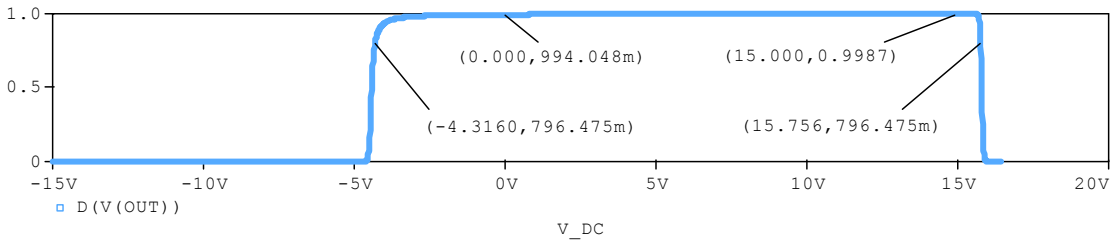

FIGURE 9

PSPICE calculation of gain showing steep transition of the gain to 1V/V as the input takes the transistor out of cutoff; at the high voltage end, the transistor can go past the onset of saturation by 756 mV before the gain suffers: that is, V_{SAT} is 756 mV, not zero as assumed in this problem

2. Show how $\upsilon_{OUT}(t)$ is constructed for $\upsilon_{IN}(t)$ using the DC transfer characteristic.

ANSWER

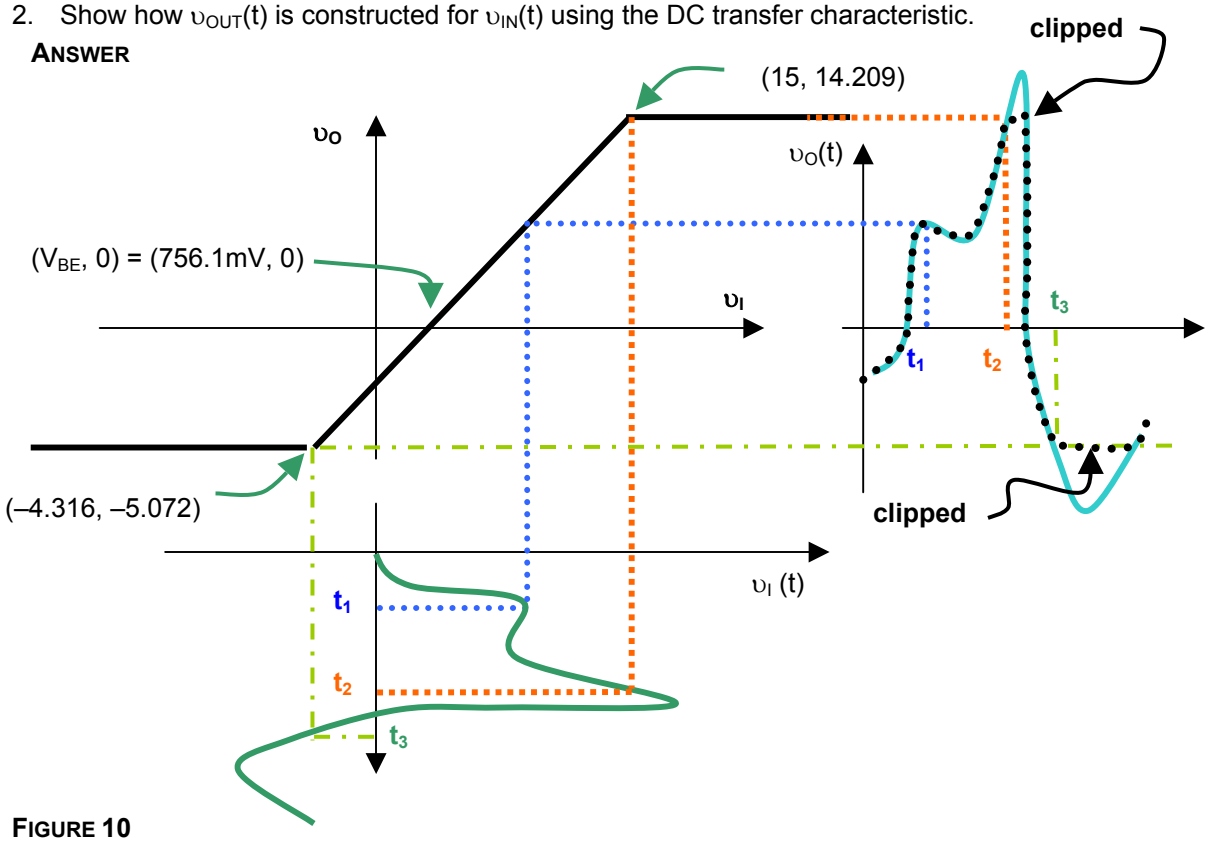

FIGURE 10

Construction of output waveform using DC input-output transfer function

The V_{BE}-offset of the transfer function along the x-axis causes the output waveform to translate downward in voltage ($\upsilon_O = \upsilon_I - V_{BE}$). Selecting a time t_1 on the input waveform, corresponding voltage $\upsilon_I(t_1)$ is tracked upward to the υ_I-axis of the transfer plot. The corresponding υ_O is found from the transfer curve and plotted on the output waveform at the same time t_1. Where the transfer curve has zero gain, all input waveform points in the zero gain region plot at the same output level in the output waveform, causing clipping of the output waveform. Examples are clipping at time t_2 on the upswing at 14.209 V, and at time t_3 on the downswing at –5.072V.

3. Plot one cycle of the output waveform, labeling all corner voltages and times.

ANSWER

See Figure 11.

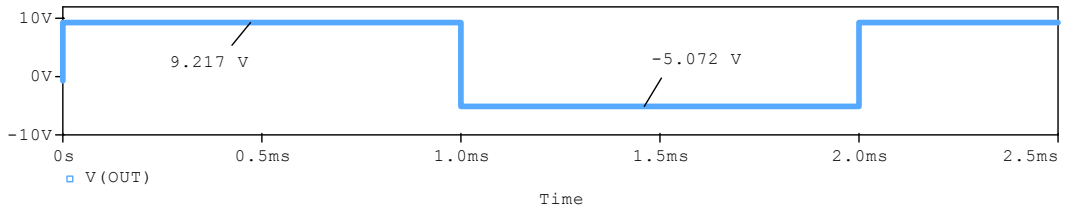

FIGURE 11

Output waveform for a square wave input $\upsilon_I(t) = 10\ sq(t)$; for hand analysis, the value of V_{BE} at zero output voltage is used, making the maximum voltage from hand analysis υ_O = 9.24 V instead of the PSPICE value 9.22V

OUTLINE

At $\upsilon_I = 10V$, $\upsilon_O = 10V – V_{BE} = 10 – 756.1mV = 9.24V$. At $\upsilon_I = –10V$, the VF cuts off and υ_O = min V_O = –5.07 V

4. Express the output waveform as a DC part plus a transient part that has zero time average over a cycle. That is, $\upsilon_{OUT}(t) = V_{DC} + V_{AC} sq\ (t)$

ANSWER

$$\upsilon_{OUT}(t) = 2.09 + 7.16\ sq\ (t).$$

OUTLINE

At the positive maximum, $V_{DC} + V_{AC} = 9.24V$. At the negative minimum, $V_{DC} – V_{AC} = –5.07V$. Adding these two equations, $V_{DC} = (9.24–5.07)/2 = 2.09$ V. Subtracting them, $V_{AC} = (9.24+5.07)/2 = 7.16$ V.

5. Calculate the power efficiency counting only the output power related to the transient voltage $V_{AC} sq(t)$ as useful power.

ANSWER

$$\eta = 19.7\%.$$

OUTLINE

Useful power is the AC output power. Since the AC output voltage is the same in both halves of the cycle,

EQ. 5

$$P_{USEFUL} = V_{AC}^2/R_L = 7.16^2/100 = 512\ mW.$$

The power input to the circuit (neglecting the base current contribution) has two parts. The instantaneous input from the positive voltage source is $p_P(t) = V_P\ \iota_C(t)$, with the instantaneous current

EQ. 6

$$\iota_C(t) = \beta\iota_E(t)/(\beta+1) = \frac{\beta}{\beta+1}\left(I_M + \frac{\upsilon_O(t)}{R_L}\right) = \frac{\beta}{\beta+1}\left(I_M + \frac{V_{DC} + V_{AC} sq(t)}{R_L}\right).$$

Integrating over a cycle, the *sq* (t) averages to zero as it has equal up and down swings. Therefore, the average DC input power is

EQ. 7

$$P_P = \frac{\beta}{\beta+1}\left(I_M + \frac{V_{DC}}{R_L}\right)V_{CC} = \frac{50}{51}\left(5.07 + \frac{2.09}{100}\right)15 = 1.053\ W$$

The current to the negative source all comes from the mirror, which carries a constant DC current. The emitter currents of both Q2 and Q3 flow through the negative source, so the power input from the negative supply is given by EQ. 8 below.

EQ. 8

$$P_N = (1+1/\beta)\, 2I_M\, V_{CC} = 1.552\ \text{W}$$

Therefore, the amplifier efficiency is

EQ. 9

$$\eta = \frac{P_{useful}}{P_N + P_P} = \frac{512\text{mW}}{1.053 + 1.552} = 19.7\%.$$

Problem 2: Class AB amplifier

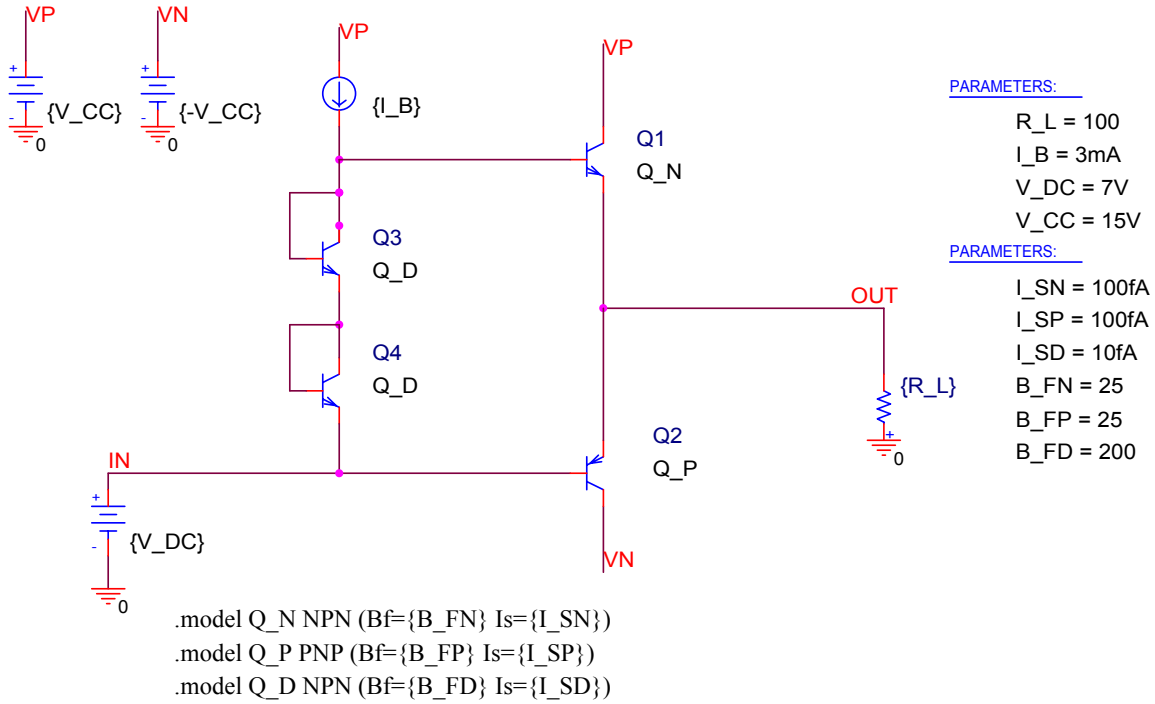

FIGURE 12

Class AB amplifier; Early voltage is infinity for all transistors

In the following, first derive a FORMULA for the answer using only variables (no numbers); then EVALUATE your formula.

For the parameters given in Figure 12 determine:

1. The emitter current of Q1 when the output voltage is zero

ANSWER

$$I_Q = \frac{I_B}{\frac{1}{\beta_N + 1} + \frac{(1+1/\beta_D) I_{SD}}{(1+1/\beta_N) I_{SN}}} = 22.2\ \text{mA}$$

OUTLINE

The base-to-base voltage is

EQ. 10

$$V_{BB} = 2V_{TH}\ell n\left(\frac{I_B - \frac{I_Q}{\beta_N + 1}}{(1+1/\beta_D) I_{SD}}\right) = V_{TH}\ell n\left(\frac{I_Q}{(1+1/\beta_N) I_{SN}}\right) + V_{TH}\ell n\left(\frac{I_Q}{(1+1/\beta_P) I_{SP}}\right) = 2V_{TH}\ell n\left(\frac{I_Q}{(1+1/\beta_N) I_{SN}}\right)$$

where the last step uses the fact that the NPN and PNP output transistors are matched. Because the logarithms are equal, the arguments of the logarithms are equal, so

EQ. 11

$$\frac{I_B - \frac{I_Q}{\beta_N + 1}}{(1 + 1/\beta_D) I_{SD}} = \frac{I_Q}{(1 + 1/\beta_N) I_{SN}}.$$

Solving for I_Q we find

EQ. 12

$$I_Q = \frac{I_B}{\frac{1}{\beta_N + 1} + \frac{(1 + 1/\beta_D) I_{SD}}{(1 + 1/\beta_N) I_{SN}}} = 22.2 \text{ mA}.$$

2. The maximum and minimum output voltages

ANSWER

$$\upsilon_O(\text{max}) = I_B(\beta_N + 1)R_L = 7.8 \text{ V}; \quad \upsilon_O(\text{min}) = -V_{CC} + V_{EB} = -14.28 \text{ V}.$$

OUTLINE

The maximum output voltage occurs when all of I_B is used as base current to the NPN, making the output current the largest possible. In this case the output current is $I_B(\beta_N+1)$, and if the PNP is cutoff all this current goes through the load resistor R_L, so $\upsilon_O(\text{max}) = (\beta_N+1)\, I_B\, R_L$.

The minimum output voltage occurs when $\upsilon_{IN} = -V_{CC}$, causing the PNP transistor to saturate. When $\upsilon_{IN} = -V_{CC}$, the output voltage is $\upsilon_O = \upsilon_{IN} + V_{EB}$, leading to a collector current in the PNP

EQ. 13

$$I_C = \frac{V_{CC} - V_{EB}}{(1 + 1/\beta_P) R_L};$$

With EQ. 13 we can find V_{EB} by iteration using the diode law

EQ. 14

$$V_{EB} = V_{TH} \ell n\left(\frac{I_C}{I_{SP}}\right) \rightarrow V_{EB} = 722.8 \text{ mV}, \upsilon_O(\text{min}) \text{ -= } -14.28 \text{ V}.$$

3. The small-signal gain at zero output voltage

ANSWER

EQ. 15

$$\frac{V_O}{V_S} = \frac{1}{1 + \frac{r_\pi}{(\beta_N + 1)R_L} \frac{2r_E + r_\pi}{[2r_E + 2r_\pi]}} = 0.993 \text{ V/V},$$

where r_E = diode-connected transistor resistance and r_π = NPN output transistor input resistance.

OUTLINE

The value of r_E is found using

EQ. 16

$$r_E = \frac{V_{TH}}{I_E(\text{diode})} = \frac{V_{TH}}{I_B - \frac{I_Q}{\beta_N + 1}} = 12.05\ \Omega.$$

The value of r_π is found using

EQ. 17

$$r_\pi = \frac{\beta_N V_{TH}}{I_C(\text{NPN})} = \frac{(\beta_N + 1) V_{TH}}{I_Q} = 30.28\ \Omega.$$

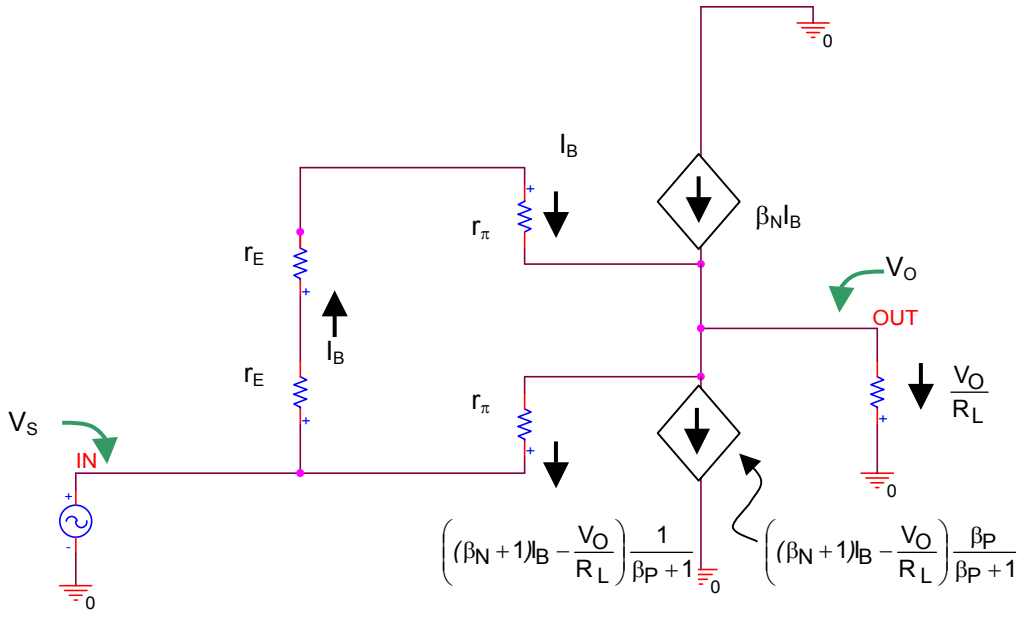

FIGURE 13
Small-signal circuit for gain analysis

The small-signal circuit is shown in Figure 13. KVL along the bottom of Figure 13 provides EQ. 18 below.

EQ. 18

$$V_S = V_O - \left((\beta_N+1)I_B - \frac{V_O}{R_L}\right)\frac{r_\pi}{\beta_P+1}.$$

KVL around the interior loop provides

EQ. 19

$$I_B(2r_E+r_\pi)+\left((\beta_N+1)I_B-\frac{V_O}{R_L}\right)\frac{r_\pi}{\beta_P+1}=0.$$

We solve for I_B and substitute the result in EQ. 18 to find

EQ. 20

$$V_S = V_O\left(1+\frac{r_\pi}{(\beta_P+1)R_L}\left(\frac{2r_E+r_\pi}{2r_E+\left(1+\frac{\beta_N+1}{\beta_P+1}\right)r_\pi}\right)\right).$$

Because the transistors are matched, $\beta_N = \beta_P$ and EQ. 20 leads to EQ. 15.

4. If only B_FN is varied, what value of B_FN will result in a positive output level for V_{IN} = 7.5 V equal in magnitude to the negative output level for V_{IN} = –7.5V?

ANSWER

EQ. 21

$$\beta_N = \frac{V_O}{I_B R_L} - 1 = 21.65$$

OUTLINE

On the positive swing, the diodes raise the base of the NPN by $2V_D$ and the NPN drops the output by V_{BE} below the base. Hence, the output will be $V_O = V_I + 2V_D - V_{BE}$.

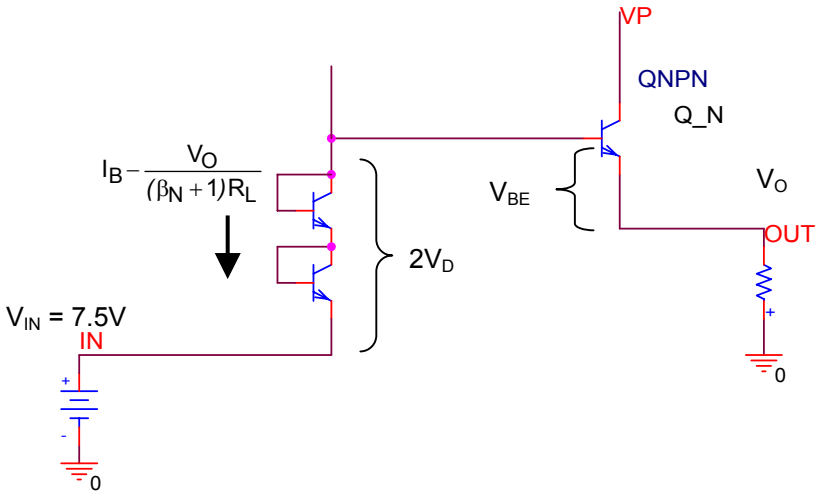

FIGURE 14

On positive swing $V_O = V_{IN} + 2V_D - V_{BE} = 7.5 + 2V_D - V_{BE}$

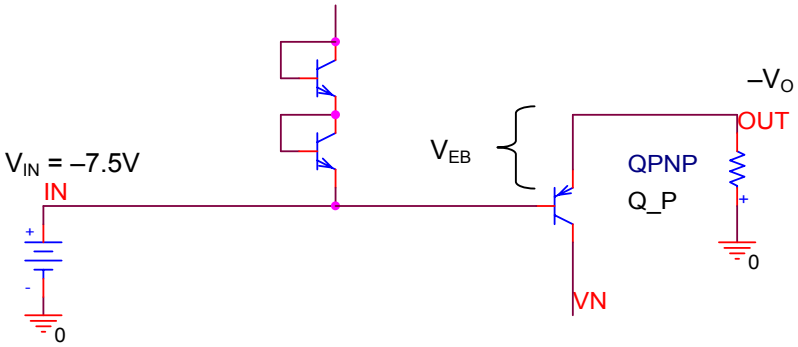

FIGURE 15

On negative swing, $-V_O = V_{IN} + V_{EB} \rightarrow V_O = 7.5 - V_{EB}$

On the negative swing, the diodes have no effect and the input is V_{EB} below the output. We set the output voltages to be V_O for positive input and $(-V_O)$ for negative input, which makes both load currents V_O/R_L the same. That means for matched transistors V_{EB} (negative input) = V_{BE} (positive input). Therefore, for matched transistors we will get the same V_O for the same input V_{IN} (except for sign) only if $V_D = 0$. To get zero diode drop we need zero diode current. [1]
Consequently, zero V_D implies β_N should be chosen so

EQ. 22

$$I_B = \frac{V_O}{(\beta_N + 1)R_L},$$

or, see EQ. 23 below:

EQ. 23

$$\beta_N = \frac{V_O}{I_B R_L} - 1 = 21.65$$

With this value of β_N, the diode voltage is zero, but the NPN transistor V_{BE} has changed to EQ. 24 below.

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[1] The current and diode voltage are related by $I_D = I_S\left(e^{\upsilon_D / V_{TH}} - 1\right) \rightarrow 0$ as $\upsilon_D \rightarrow 0$ V.

EQ. 24

$$V_{BE} = V_{TH}\ell n\left(\frac{V_O / R_L}{(\beta_N + 1) I_{SN}}\right) = V_{BE}(\beta_N = \beta_P) + V_{TH}\ell n\left(\frac{\beta_P + 1}{\beta_N + 1}\right) = V_{BE}(\beta_N = \beta_P) + 0.0036V\ ,$$

where $V_{BE}(\beta_N=\beta_P)$ is the NPN V_{BE} for the case of matched transistors with $\beta_N = \beta_P$. EQ. 24 shows a small increase in V_{BE} because of the change in β_N, which no longer is the same as β_P, but smaller. This increase in V_{BE} means we need to increase the diode drop above zero to a few mV to compensate for the change in β_N, but this correction in V_D according to the diode law is not significant, corresponding to only a change in current about the same size as the scale current of the diodes.

It turns out that a more serious error is the assumption that the NPN completely cuts off when the negative voltage is applied. It does not completely cut off, but correcting this error also causes little change in β_N, as seen in the PSPICE results of Figure 16 and Figure 17 below.

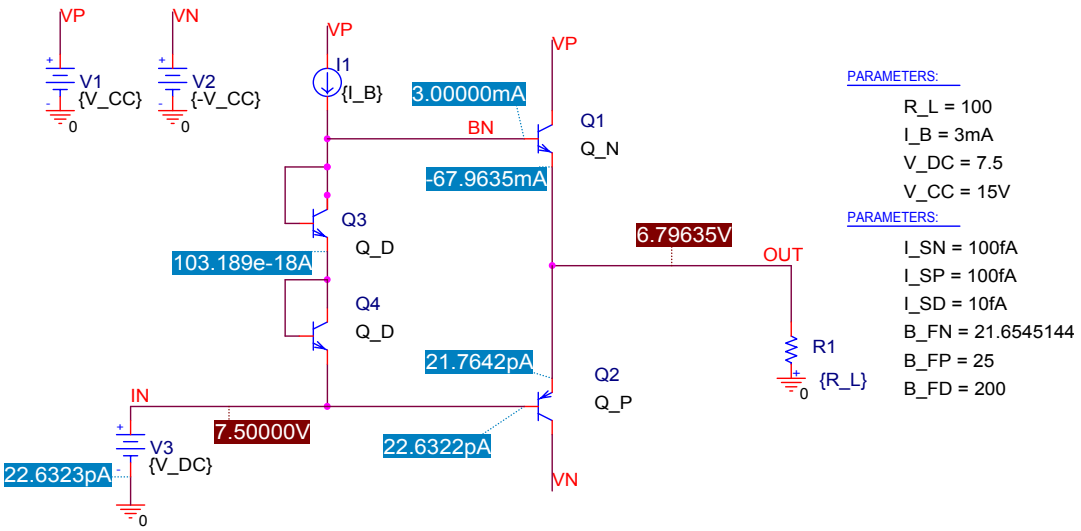

FIGURE 16

PSPICE output for input voltage of 7.5 V; PNP and diode-connected transistors are cutoff, as assumed

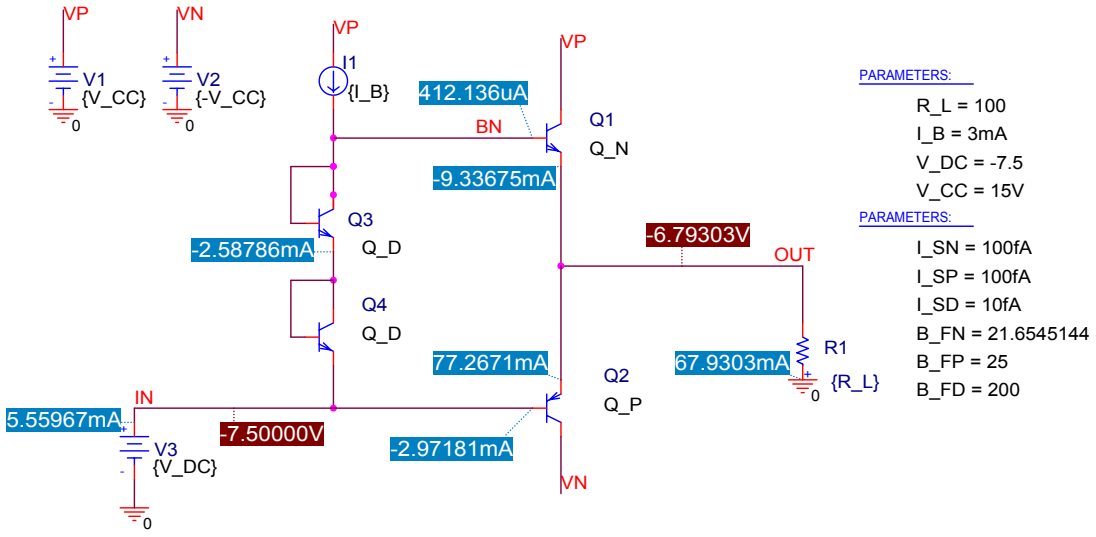

FIGURE 17

PSPICE output for input voltage of –7.5 V; NPN transistor is not cutoff, contrary to our assumption, but the output voltage is 6.793V, very close to 6.796 V from Figure 16