High-Q micromachined resonant cavities in a K-band diplexer configuration

M.J.Hill, J.Papapolymerou and R.W.Ziolkowski

Abstract: Microwave diplexers are often used in transmit/receive systems to isolate a power transmit stage from a sensitive receive stage sharing a common antenna. For efficient bandwidth usage and optimum antenna performance, the transmit/receive frequencies are typically placed close together in the frequency spectrum. With today's requirements for high performance, small-size wireless devices, diplexers exhibiting close channel spacing, low insertion loss and small channel bandwidths are increasingly necessary. Utilising two high-Q micromachined silicon cavity resonators, a planar K-band diplexer has been designed, fabricated and tested. This diplexer shows transmit/receive bandwidths of 1.11 and 1.53% and insertion losses of 1.4 and 1.0dB, respectively. Channel centre frequencies of 18.64 and 20.47GHz provide a channel separation of approximately 9%, and channel-to-channel isolation greater than 26dB over the entire measured frequency range. The diplexer can be accessed via microstrip lines and can be easily integrated with other planar circuits and structures, such as mixers, amplifiers, oscillators and patch antennas. The proposed design is the first step towards a more mature multi-pole diplexer with enhanced overall performance.

1 Introduction

The rapid expansion and growth of wireless communication systems for military and commercial applications has led to a dramatic increase in the implementation of microwave and mm-wave systems. Commercial applications of these systems include short-haul line-of-sight transmission links for personal communication networks (PCNs) that operate at 38GHz, wireless cable at 28GHz, wireless local area networks (LANs), automotive anti-collision radar at 77GHz and mobile broadband systems [1].

Microwave and millimetre-wave components are traditionally built with waveguide technology that offers low-loss and high quality factor circuits at the price of large size and weight, high cost, incompatibility with monolithic circuits and increased fabrication complexity especially at higher frequencies [2]. For commercial systems, however, high-yield, increased component density, small size and low cost are fundamental requirements that need to be met. Traditional silicon fabrication has met these requirements for low frequency devices, but because of silicon's low electron mobility, has had limited success for high frequency devices. However, new silicon technologies are increasing the useful frequency range of active silicon devices, and promise to provide future high frequency devices many of the advantages of traditional silicon processing. Additionally, the availability of micromachining techniques that are compatible with silicon processes will aid in the develop-

ment of these low-cost, high frequency circuits by allowing the placement of mechanical and waveguide-like microwave structures on the same substrates as active silicon devices.

One of the major limiting waveguide components of microwave/mm-wave wireless communication systems is the transmit/receive diplexer that is used to provide low-insertion loss and high channel-to-channel isolation. Realisation of the diplexer with planar resonators and filters is generally avoided due to their low quality factors and to the higher losses of the resulting circuits that are caused by the presence of the substrate material. With recent developments in microwave micromachining, however, it is now possible to make microstrip or CPW line resonators suspended on membrane [3, 4], as well as cavity resonators [5, 6] and dielectric resonators [7] that offer low-loss, high-Q and narrow bandwidth and that can be monolithically integrated with other passive components and active devices on a single chip. These advances have led to the development of high performance, suspended microstrip based K-band diplexers exhibiting 5-6.5% bandwidths and 0.9-1.4dB insertion losses [3]. This paper presents a novel approach for a planar K-band silicon diplexer with micromachined high-Q cavities.

2 Theory

In order to separate two closely spaced frequency channels, diplexers utilise two narrow band filters. The silicon diplexer presented here achieves the channel separation using two micromachined planar microstrip coupled cavity resonators or one-pole filters. Microstrip coupled resonators (see Fig. 1) have been shown to provide high-Q response at microwave frequencies [5]. They consist of one silicon micromachined cavity, two microstrip lines for input and output, and two slots that couple energy magnetically from the microstrip lines into the cavity. To maximise this

IEE Proc.-Microw. Antennas Propag., Vol. 148, No. 5, October 2001

307

magnetic coupling, a short is placed at the centre of each slot by using quarter-wavelength long open circuited stubs beyond the slot centres. The coupling coefficient between the microstrip lines and the cavity can also be controlled by the size and location of the slots [5, 8]. Because of their performance and ease of integration, these one-pole filters are ideally suited for preliminary testing of a micromachined cavity diplexer. We should mention here that a multi-pole diplexer design is also possible by using several cavities interconnected with coupling slots. The inter-resonator coupling can be controlled by the size of the slots and their location relative to the two cavities.
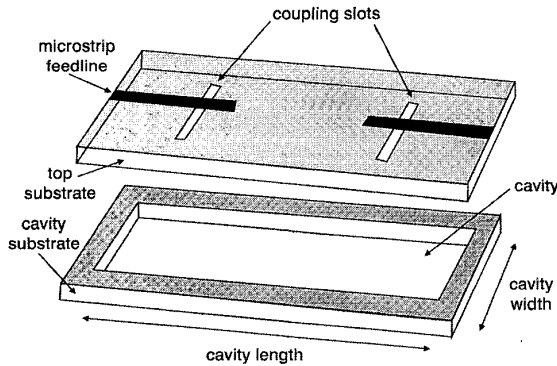

Fig. 1 *Microstrip coupled resonant cavity*

Currently there is interest in the use of the K-band for point-to-point communications and wireless LANs [9]. The frequencies selected for the diplexer design, $F_1 = 19\,\text{GHz}$ for the receive channel (channel 1) and $F_2 = 21\,\text{GHz}$ for the transmit channel (channel 2), are in this band. Because the resonant frequency of the fundamental TE_{101} mode in a cavity of length L_{cavity}, width W_{cavity} and height H_{cavity} is

$$f_{res} = \frac{c}{2\pi} \sqrt{\left(\frac{\pi}{L_{cavity}}\right)^2 + \left(\frac{\pi}{W_{cavity}}\right)^2} \quad (1)$$

the length and width for the two rectangular cavities of the diplexer were selected to be [10]: $W_{cavity1} = 8.01\,\text{mm}$ and $L_{cavity1} = 17.5\,\text{mm}$ for the channel 1 cavity, and $W_{cavity2} = 8.85\,\text{mm}$ and $L_{cavity2} = 15.83\,\text{mm}$ for the channel-2 cavity. The height of both cavities was $H_{cavity1,2} = 1.0\,\text{mm}$. Other cavity parameters, such as the coupling slot length and width were chosen as described in [2].

The topology chosen for the silicon diplexer is shown in Fig. 2. This design utilises a microstrip T-junction to connect the two resonant cavities of the diplexer. The design of the microstrip lines connecting the T-junction to the resonant cavities is critical for proper operation of the diplexer. Specifically, it is important that the lengths L_1 and L_2 be adjusted to reflect an open circuit at the T-junction at the resonant frequencies of the channel 2 and channel 1 cavities, respectively, for the T-junction to operate effectively (see Fig. 2). This is accomplished by setting the transmission line lengths L_1 and L_2 according to eqn. 2:

$$L_1 \simeq \frac{n\lambda_{g2}}{2}, \quad L_2 \simeq \frac{n\lambda_{g1}}{2} \quad (2)$$

where $\lambda_{g1} = c/(f_{res1}\sqrt{\varepsilon_e})$ and $\lambda_{g2} = c/(f_{res2}\sqrt{\varepsilon_e})$ are the effective resonant wavelengths of the channel-1 and channel-2 cavities, respectively, f_{res1} and f_{res2} are the resonant frequencies of the channel 1 and channel 2 cavities, respectively, ε_e is the effective dielectric constant of the microstrip lines, and c is the speed of light.
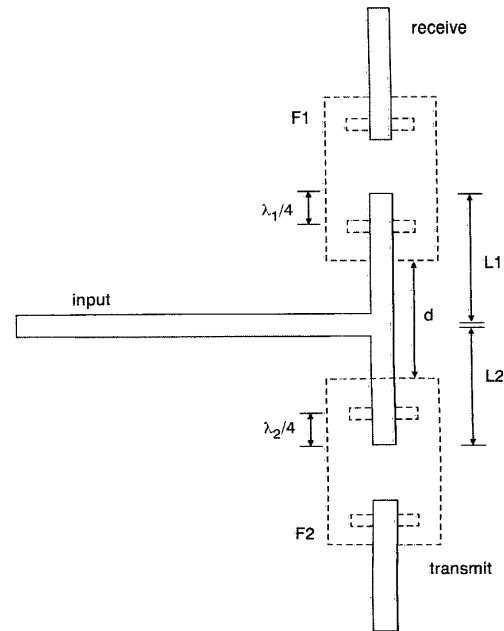

Fig. 2 *Diplexer topology*

The equations in eqn. 2 are only approximations because in practice one must compensate for the open-end effects of the feed stubs. In most cases it is desirable to design the transmission line lengths L_1 and L_2 with the integer $n = 1$ in the equations in eqn. 2, as this provides the smoothest out of band performance. Often, however, it is not possible to implement the diplexer with $n = 1$. The separation between cavity walls, d, becomes negative if:

$$\sqrt{\varepsilon_e} > \frac{4c}{L_{cavity1} + 4\delta_{min}} \left(\frac{1}{2f_{res2}} - \frac{1}{4f_{res1}}\right) \quad (3)$$

where δ_{min} is the minimum manufacturable distance between the two cavities and $L_{cavity1}$ is the length of the first cavity.

Physically, a negative value for d results in cavity overlap that would prevent the proper operation of the resonant cavities. In these situations, the transmission line lengths L_1 and/or L_2 must be increased by setting $n > 1$ in the equations in eqn. 2. However, for $n > 1$ the transmission line lengths L_1 and L_2 will reflect open circuits to the T-junction at frequencies other than the resonant frequency of the two cavity resonators. Ripples in the response of the diplexer will then result. These ripples can be severe and as n gets large and can begin to overlap with the cavity resonance, resulting in very poor performance [11]. Typically, setting $n = 2$ results in a good compromise between performance and a non-physical solution. An alternative solution to this problem is to design the diplexer in a configuration where the two cavities are on different planes (3-D implementation) and are fed by a stripline between those planes. The silicon diplexer discussed in this paper was designed with $n = 2$ for both cavity feeds. Figs. 3 and 4 show the electric field plots obtained with ANSOFT's high frequency structure simulation (HFSS) software, a finite element method (FEM) based full wave Maxwell equation solver, for the diplexer operating at 19 and 21 GHz, respectively. The open circuits reflected to the T-junction by the non-resonant cavity feeds can be seen clearly.
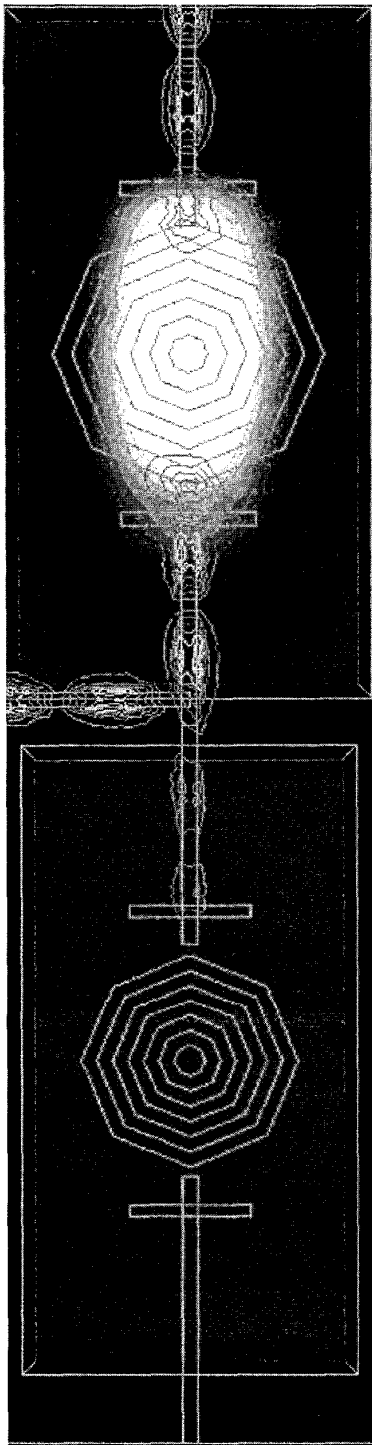
308

IEE Proc.-Microw. Antennas Propag., Vol. 148, No. 5, October 2001

Fig. 3 *Electric field plot at f = 19 GHz*

3 Diplexer design and fabrication

Initially the diplexer circuit was implemented on Rogers Duroid as a test for the final silicon construction [11]. The cavities for this test circuit were mechanically machined in an aluminum test fixture that was secured to the Duroid substrate with plastic screws and a clamp. Although this device was used as a guide for silicon construction and exhibited very good performance [11], several significant differences exist between the Duroid and silicon diplexers.
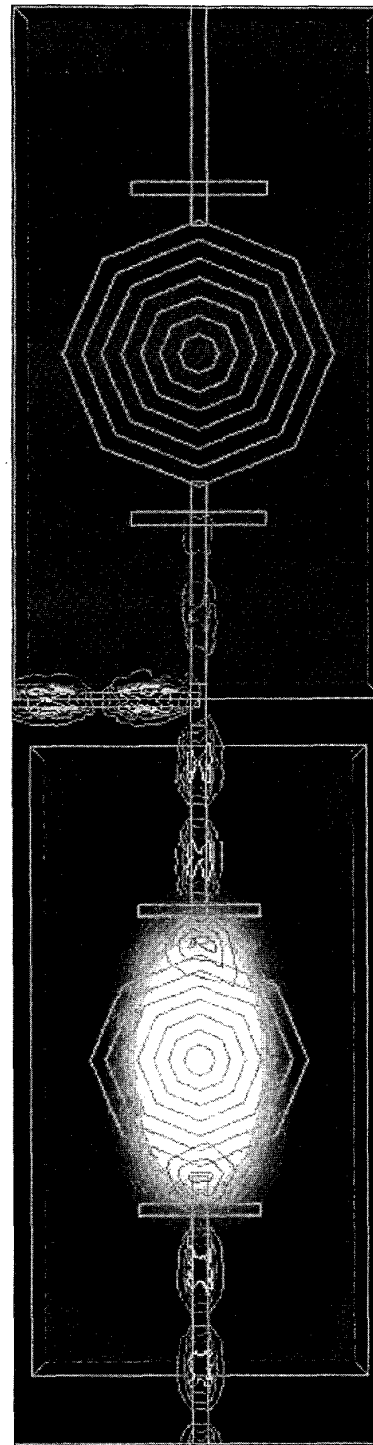

Fig. 4 *Electric field plot at f = 21 GHz*

The silicon diplexer was fabricated using a stack of three silicon wafers. The top wafer served as a substrate for the microstrip feed lines. In order to minimise microstrip loss, a high resistivity ($\rho > 1000\,\Omega$-cm) 400 μm thick silicon wafer was used. The design also included CPW-to-microstrip transitions to allow for on-wafer probing and measurement of the diplexer. These transitions are not part of the diplexer and, thus, do not have to be included in a microstrip-based microwave system realisation. The second and third wafers were low resistivity 1 mm thick wafers with a

IEE Proc.-Microw. Antennas Propag., Vol. 148, No. 5, October 2001

309

<1-0-0> crystal orientation. These wafers were used to define the resonant cavities. The cavities were micromachined in the second wafer through a chemical wet etch with tetramethylammonium hydroxide (TMAH) [12]. The third wafer was used to seal the bottom of the etched cavity (see Fig. 5). The TMAH wet etch provides an anisotropic etch; and when used on <1-0-0> silicon, results in a cavity with sloped (54.74 degrees) side-walls (see Fig. 6). This presents a problem with respect to the resonant frequency described by eqn. 1. The sloping side-walls can perturb the resonant frequency significantly. If the cavity is designed, however, to maintain a volume similar to the ideal vertical wall case, then the resonant frequency can be well approximated by eqn. 1. Further optimisations can then be performed using three-dimensional modelling tools such as Ansoft's HFSS.
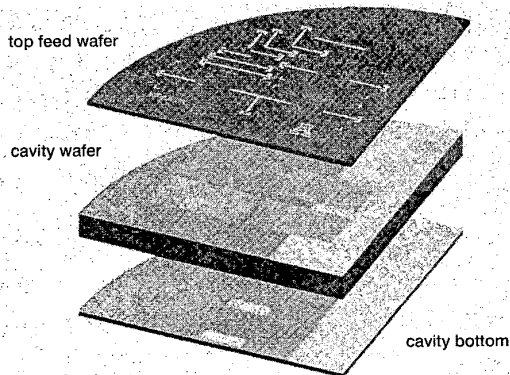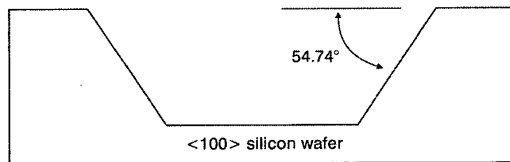

Fig. 5 *Diplexer wafer stack*

Fig. 6 *Anisotropic silicon etch*

Following optimisation of the cavity resonators, feed stubs, and T-junction with HFSS, the diplexer was fabricated using standard silicon micromachining and lithography techniques. Because the coupling slots were required in the cavity lid, metallised circuit features were required on both the top and bottom of the top feed wafer. The coupling slot features on the bottom of the top wafer were produced through a lift-off process, and were aligned to the features on the top of the second wafer through the use of an MJB-3 mask aligner with infrared capability. This mask aligner was also used to print the cavity openings on the second wafer. These openings were then replicated in a thick oxide layer (~0.7μm) on the cavity wafer. The patterned oxide layer was then used as a mask for the TMAH etch process. When the TMAH etch process was complete, the bottom wafer was attached to the cavity wafer with conductive epoxy. This assembly was then metalised with gold to a thickness of approximately 3μm. Finally, the cavity wafer was bonded to the feed wafer with conductive epoxy. The alignment of these two structures was performed using an infrared wafer aligner and bonder. A photo of the fabricated silicon wafers is given in Fig. 7. The overall diplexer size is 37mm × 10.3mm × 2.5mm. In order to measure the quality factor of the cavity resonator, a separate single cavity with narrow coupling slots was also

fabricated on the same wafer (W_{cavity} = 8.85mm, L_{cavity} = 15.83mm), along with some calibration standards (see Fig. 7).
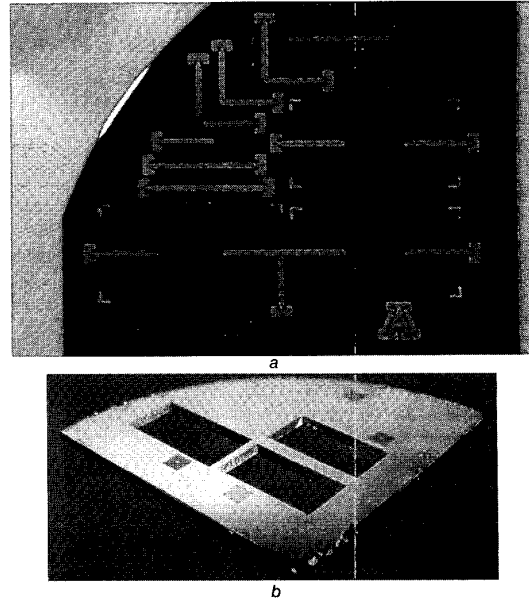

Fig. 7 *Fabricated circuits. (a) Top wafer with feeding structure and calibration standards and (b) micromachined cavities on silicon before metallisation*

4 Results

The fabricated diplexer was measured using an HP8510 network analyser and a Cascade Microtech probe station with 150μm pitch Picoprobe coplanar wafer probes. Since the network analyser can only measure a two-port circuit, the third port of the diplexer was always terminated with a 3.5mm broadband load connected to the station's third coplanar probe. De-embedding of the CPW-to-microstrip transitions was performed using on-wafer thru-reflect-line (TRL) standards and NIST's Multical software [13]. The reference planes for the 2-port measurements were located 5.78mm away from the CPW-to-microstrip transition. For insertion loss measurements the diplexer input was located right at the T-junction, while the diplexer outputs were located at the centre of the output coupling slots. For the channel-to-channel isolation measurement the reference planes were located at the centres of the input and output coupling slots.

Although the device is capable of handling significantly higher powers, due to equipment limitations, a maximum input power of approximately −5dBm was used for all measurements. The power handling capability of the device is limited mainly by dielectric breakdown within the cavity, and is therefore strongly dependent on the cavity geometry. Operation at higher power levels could increase the operating temperature of the device. Equipment limitations did not allow for an in depth study of the effects of temperature variations on the diplexer operation, however, an investigation of temperature effects has been reported on silicon cavity resonators similar to those used here [2]. The results found in [2] suggest that temperatures should be kept below 120°C to prevent excessive losses due to breakdown of the conductive epoxy bonding the wafers together. Additionally, it was found in [2] that the resonant frequency of the cavity resonator was extremely stable with increases in temperature. It is therefore expected that the diplexer will perform well over wide temperature variations.

310

IEE Proc.-Microw. Antennas Propag., Vol. 148, No. 5, October 2001

The quality factor, Q, of the resonators was found first by measuring the scattering parameters of a single cavity (see Fig. 8). To allow for accurate measurement of the unloaded Q of the cavity, Q_u the resonator coupling slots were designed to be narrow to provide approximately 20 dB of insertion loss at the resonant frequency of the cavity. The loaded quality factor (Q_l) of the resonator is defined as

$$Q_l = \frac{f_{res}}{\Delta f_{3-dB}} \qquad (4)$$

where f_{res} = 20.45 GHz is the resonant frequency of the cavity and Δf_{3-dB} = 26 MHz is its 3 dB bandwidth, and is found equal to 786. The external Q of the resonator, Q_e, that includes the input/output effects can be found from [5]

$$S_{21}(dB) = 20 \log_{10} \left(\frac{Q_l}{Q_e} \right) \qquad (5)$$

With S_{21} = –18.6 dB, eqn. 5 gives Q_e = 6689. Having obtained Q_e and Q_l, one can evaluate Q_u from the known relation [5]

$$\frac{1}{Q_l} = \frac{1}{Q_u} + \frac{1}{Q_e} \qquad (6)$$

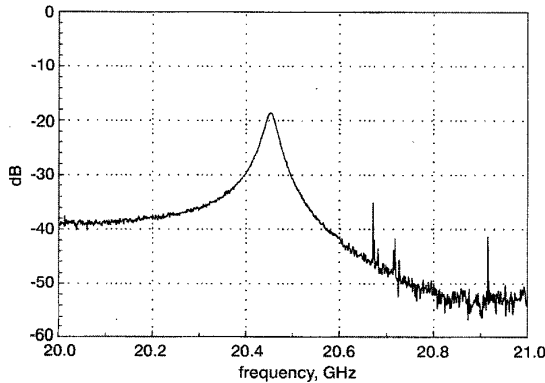Using the above definitions and the measured results, Q_u was found to be approximately 890.

Fig. 8 *Measured results of micromachined cavity resonator for extraction of unloaded quality factor*
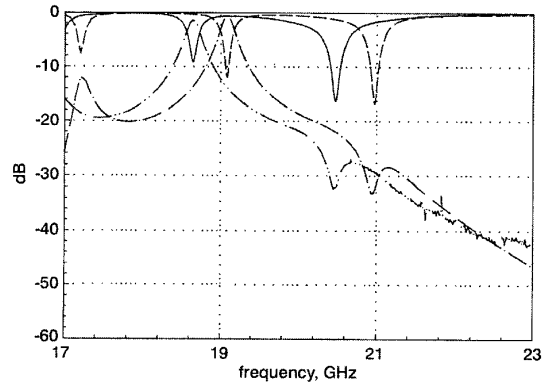

Fig. 9 *Measured and simulated results for receive channel of diplexer*
———— measured S_{11}
— — — simulated S_{11}
— — — — simulated S_{31}
— · — · measured S_{31}

Fig. 9 shows the simulated and measured results of the micromachined diplexer for the receive channel (channel 1), while Fig. 10 shows the simulated and measured results for the transmit channel (channel 2). A summary of the meas-

ured diplexer results can be found in Table 1. Figs. 9 and 10 show that there is a 2.3% shift between the simulated and measured frequencies of the diplexer. This is due to the fact that the fabricated cavities are slightly overetched and therefore larger than the ones designed. Indeed, measurement of the cavity sizes after etching indicated a 4.35% increase in the volume of both cavities (length/width increase varied from 100 to 400 μm). When this volume increase is taken into account then there is very good agreement between simulated and measured results (an increase in cavity size results in a frequency decrease), as shown in Fig. 11. In order to avoid this size increase, a compensation in the mask design can be implemented based on the TMAH solution and etch time that are used. From Fig. 9 we see that the measured insertion loss for channel 1 is 1.4 dB, which is slightly higher than the simulated value, while the return loss increased from –18 dB to –10 dB. The measured bandwidth was 1.11%, slightly smaller than the simulated result. The insertion loss for channel-2 was measured to be 1 dB, while the return loss was –18 dB, a 6 dB decrease from the simulated value. The bandwidth for channel 2 was measured to be 1.53%. The insertion loss of channel 1 was a bit higher than that of channel 2 since its return loss was also a bit higher than that of channel 2 (–10 dB compared to –18 dB). The discrepancy between the measured and simulated insertion and return loss values is partly due to the T-junction design that was optimised for the original resonant frequencies and not the actual overetched ones. If one takes into account the cavity size increase, then the feeding network can be fine-tuned for minimisation of losses and reflections at the actual resonant frequencies. Also, the simulated insertion loss did not include the CPW-to-microstrip transition (reference planes were further away from the slots). Nonetheless, it did include the silicon dielectric loss and the conductor loss for the bottom and the side-walls of the cavity. The microstrip feeding lines and their ground plane were assumed to be perfect electric
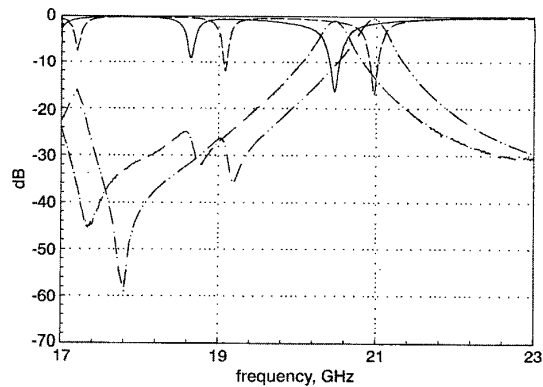

Fig. 10 *Measured and simulated results for transmit channel of diplexer*
———— measured S_{11}
— — — simulated S_{11}
— · — · measured S_{21}
— · · — · · simulated S_{21}

Table 1: Summary of silicon diplexer results

	Simulation		Measurement	
	Channel 1	Channel 2	Channel 1	Channel 2
Centre frequency, GHz	19.08	20.94	18.64	20.47
Bandwidth, %	1.33	0.96	1.11	1.53
Insertion loss, dB	0.6	0.4	1.4	1.0
Isolation, dB	>27		>26	

IEE Proc.-Microw. Antennas Propag., Vol. 148, No. 5, October 2001

311

conductors. Therefore, the measured insertion loss was a bit higher due to the extra microstrip line loss between the T-junction and the internal coupling slots of the diplexer (this portion was not de-embedded). The silver epoxy bonding is also responsible for an increase in the loss, since it can have conductivity values at 20GHz that are lower than that of traditional metals such as gold or aluminum.
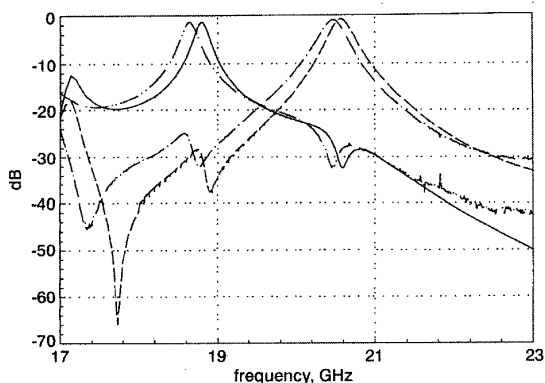

Fig. 11 *Simulated insertion loss results for both channels of diplexer with actual cavity dimensions against measured results*
——— simulated S_{31} ———— measured S_{21}
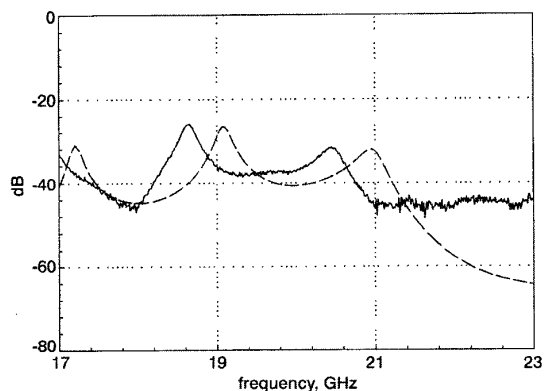— ·· — measured S_{31} — · — simulated S_{21}

Fig. 12 *Measured and simulated results for channel-to-channel isolation*
——— measured isolation
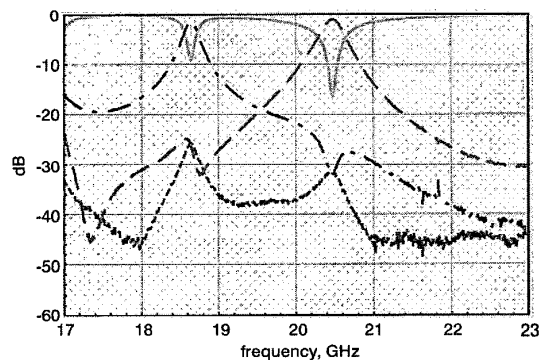——— simulated isolation

Fig. 13 *Summary of measured diplexer results*
— · — channel 1   ——— S11
——— channel 2   - - - - - isolation

Fig. 12 shows the simulated and measured results for the channel-to-channel isolation. Measurements were taken by terminating the common port (input port of the diplexer) with a 50 Ω broadband load. The measured isolation is better than 26dB across the receive band and better than 31dB across the transmit band. The measured isolation agrees fairly well with the simulated value. Although there

are some differences between measured and simulated values, overall, the results agree favourably. Additionally, it is believed that the conductive epoxy bonding technique may have resulted in increased circuit losses. Future designs could be improved by using eutectic wafer bonding techniques. All of the measurements that were performed from 17 to 23GHz are summarised in Fig. 13.

5 Conclusions

A planar micromachined cavity diplexer has been designed, fabricated and tested. The diplexer exhibited very small insertion loss (1.4 and 1dB for the receive and transmit channels, respectively), in conjunction with narrow bandwidth (1.11 and 1.53% for the receive and transmit channels, respectively) and good channel-to-channel isolation (greater than 26dB) over the entire measurement band. In addition, simulated results using Ansoft's HFSS agreed very well with measurements. The design presented in this paper is the first step towards a mature multi-pole micromachined diplexer that uses several resonant cavities to achieve a specific filter response in the transmit/receive bands and a good phase delay response. Simple integrated circuit (IC) fabrication on common silicon wafers offers the possibility of low cost, small size/weight, mass produced and easy to integrate diplexers for a multitude of applications.

6 Acknowledgments

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